

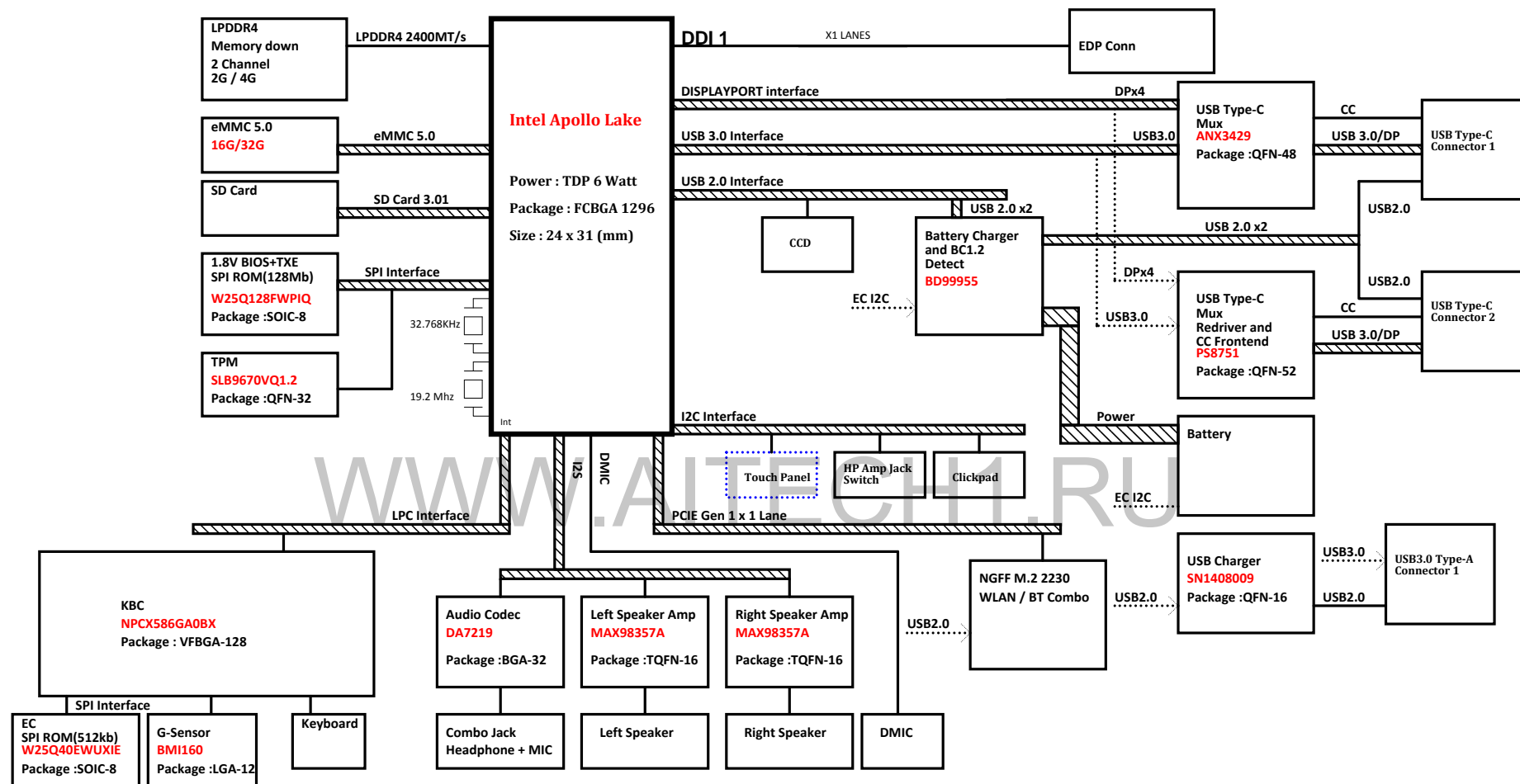
1. Schematic Page Description :

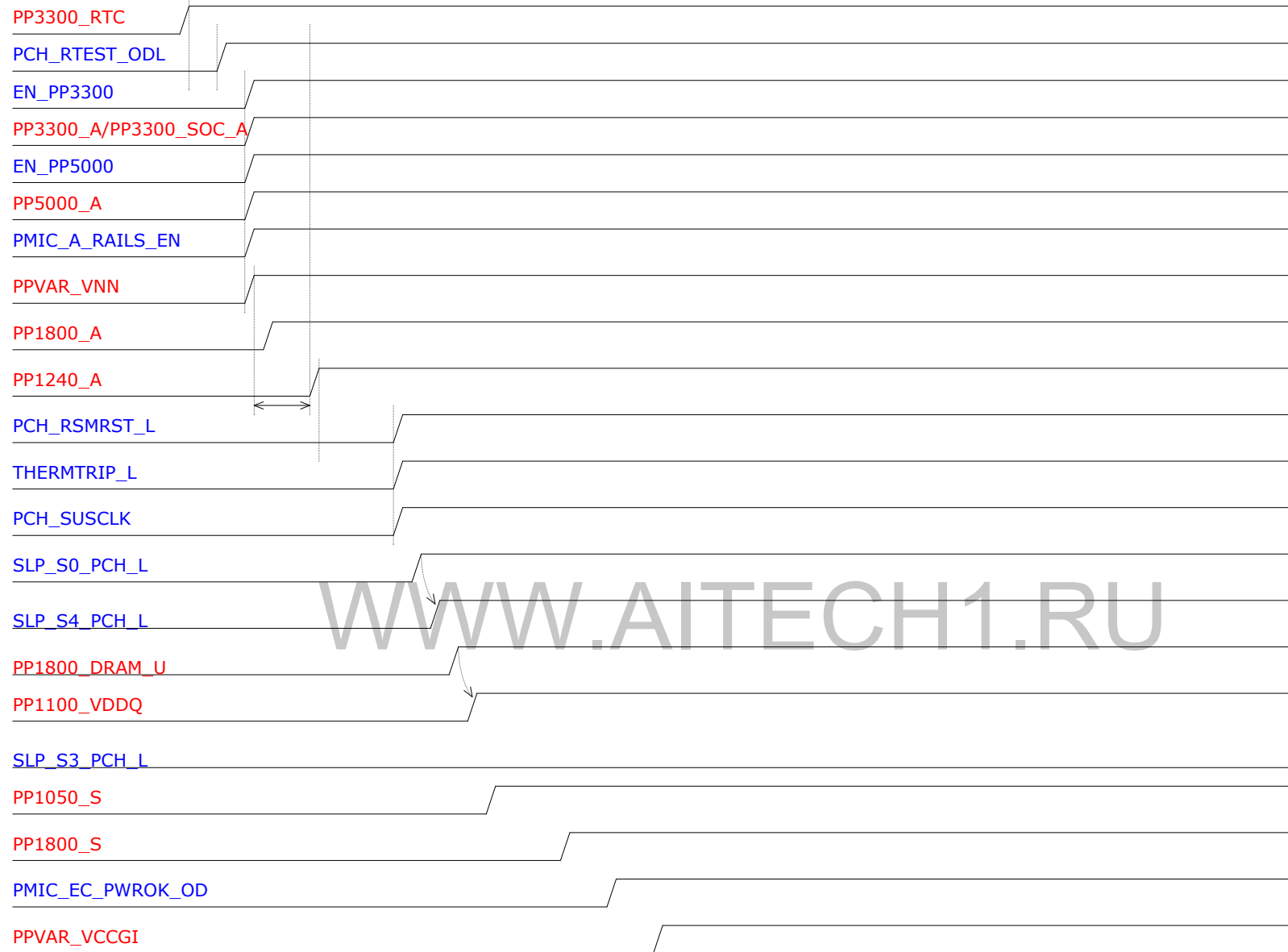
Origins Schematic Ver :

TABLE OF CONTENTS

PAGE	TITLE	PAGE	TITLE
01	Sch Page description	31	USB C ANX3429 TCPC/MUX
02	Block Diagram	32	USB C PS8751B/CONN
03	Power sequence	33	USB C 5V OUT
04	Power TREE	34	POWER---CHARGER_A49
05	APL MEMORY	35	POWER---PMIC LOGIC_A49
06	APL eDP/RCOMP	36	POWER---PMIC RAILS_A49
07	APL PCIE/USB/SATA	37	POWER: 3.3V AND 5V A49
08	APL UART/SPI/EMMC/SD/LPC	38	POWER---LOAD SWITCHES_A4
09	APL I2C/I2S/GPIO	39	INAs
10	APL PMU/JTAG	40	PTC Circuit
11	APL POWER	41	H1 SECURE MICROCONTROLLER
12	APL GROUND	42	EE A to B EC History
13	APL NO CONNECT	43	EE B to C EC History
14	MEMORY CH 00/01 LPDDR4	44	PWR A to B EC History
15	MEMORY CH 10/11 LPDDR4	45	PWR B to C EC History
16	SOC DECOUPLING		
17	SPI FLASH		
18	MIPI60 DEBUG HEADER		
19	SERVO CONNECTOR		
20	TPM/SILEGO RESET		
21	eMMC/uSD		
22	AUDIO/B CONN ,SPK AMP		
23	KB, TP, LID/B		
24	eDP,CAM,TOUCH		
25	GYRO+Accel.BMI160		
26	LED/SW		
27	NGFF WIFI/BT		
28	EC NPCX586GA0BX		
29	USB A CONNECTORS		
30	USB C CONNECTORS		

Intel Apollo Lake Platform Block Diagram

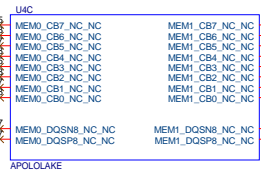




PROJECT : LI8G
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Size	Document Number	Rev
		3C
Power sequence		
Date: Monday, November 28, 2016	Sheet	3 of 45

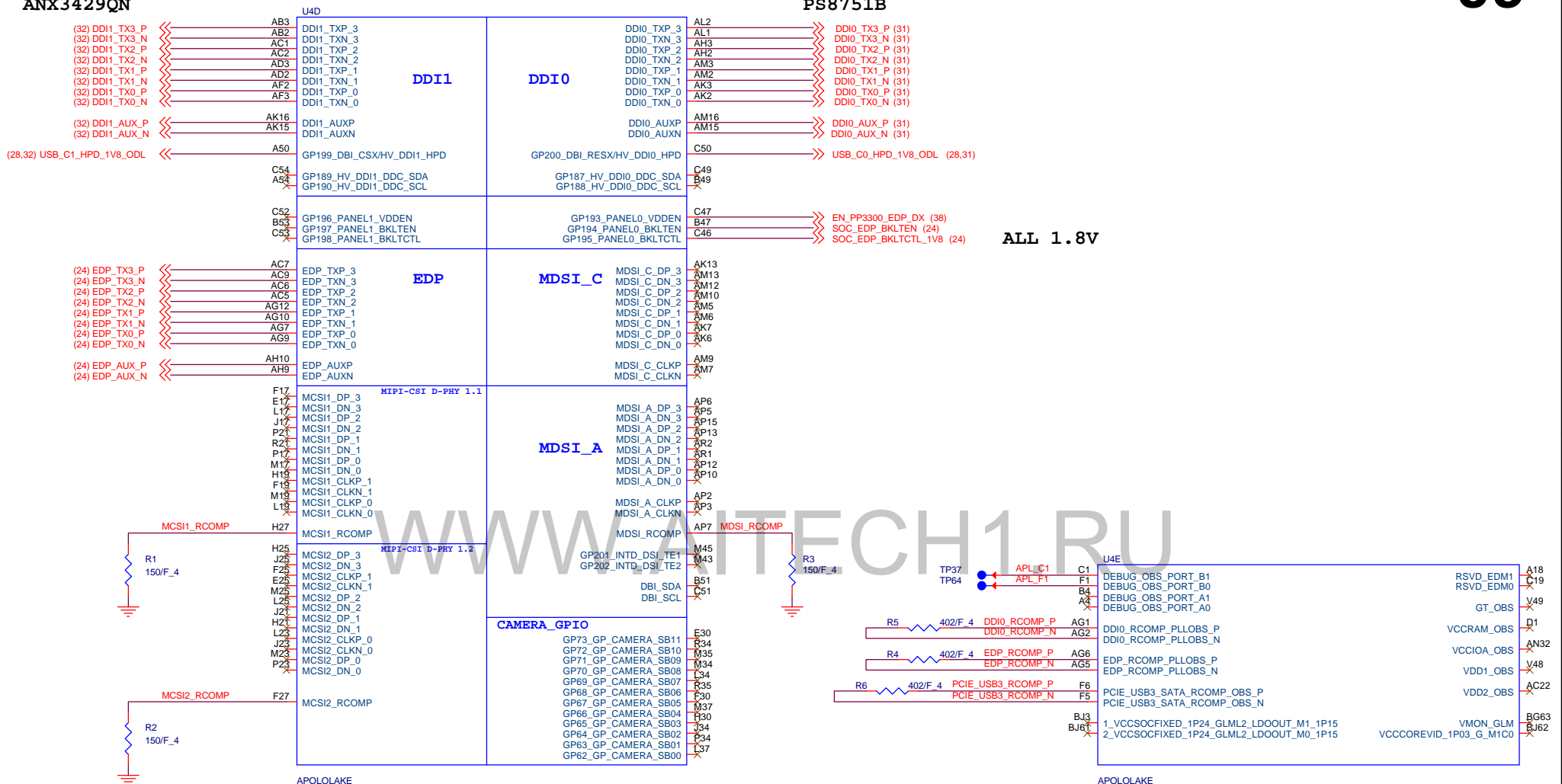
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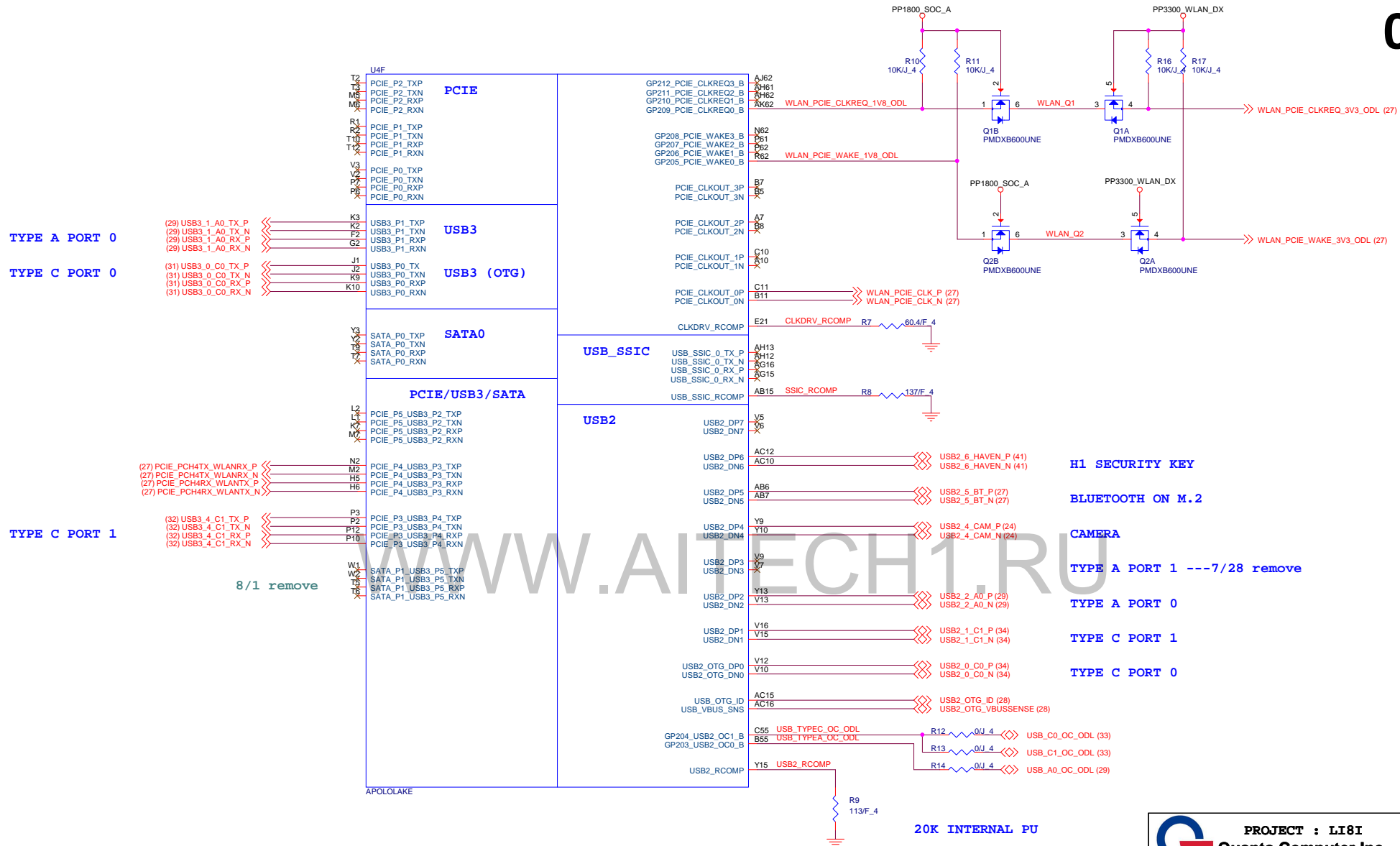


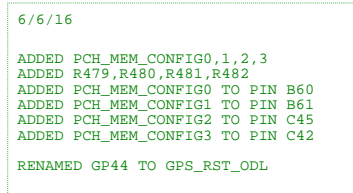
TYPE-C PORT 1
Left side
ANX3429QN

TYPE-C PORT 0
Right side
PS8751B

06

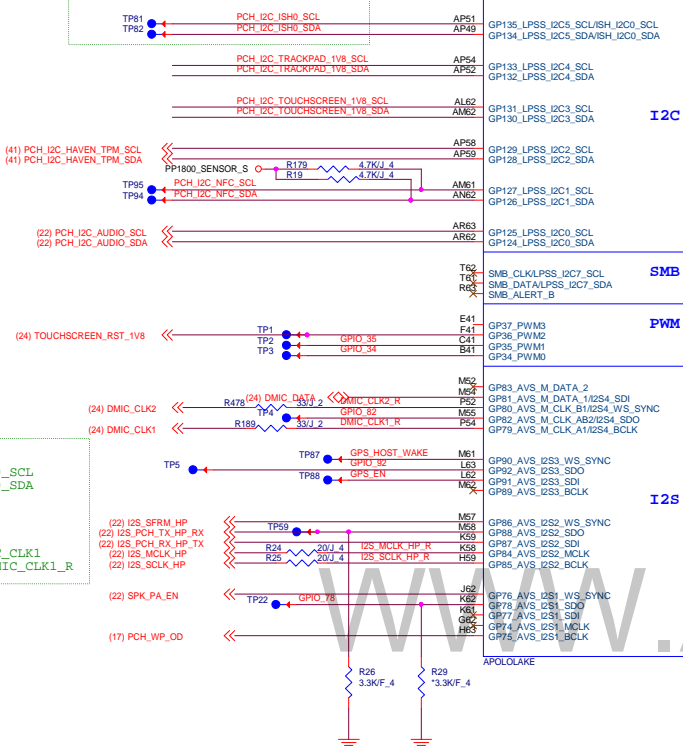






HARDWARE STRAPS (* = SYSTEM STRAP SELECTION)				
GPIO_39: INTERNAL 20K PD *DISABLE CSE ROM BYPASS: 0 ENABLE CSE ROM BYPASS: 1	GPIO_47: INTERNAL 20K PD *DON'T FORCE DNX FW LOAD: 0 FORCE DNX FW LOAD: 1	GPIO_106: INTERNAL 20K PU *MUST BE HIGH WHEN RSM_RST_N DEASSERTS	GPIO_117: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_120: INTERNAL 20K PD *TOP SWAP OVERRIDE DISABLE: 0 TOP SWAP OVERRIDE ENABLE: 1
GPIO_40: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_48: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_111: INTERNAL 20K PU DO NOT BOOT FROM SPI: 1 *BOOT FROM SPI: 0	GPIO_123: INTERNAL 20K PU MUST BE HIGH WHEN RSM_RST_N DEASSERTS	GPIO_121: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS
GPIO_43: INTERNAL 20K PU ENABLE BOOT FROM EMMC: 1 *DISABLE BOOT FROM EMMC: 0	GPIO_104: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_118: INTERNAL 20K PD *NO FLASH DESCRIPTOR OVERRIDE: 0 OVERRIDE FLASH DESCRIPTOR: 1	GPIO_112: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	
GPIO_44: INTERNAL 20K PU *ENABLE BOOT FROM SPI: 1 DISABLE BOOT FROM SPI: 0	GPIO_105: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_110: INTERNAL 20K PU LPC BUFFERS AT 1.8V: 1 *LPC BUFFERS AT 3.3V: 0	GPIO_113: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	

TP81, TP82 ON BACKSIDE



GPIO

I2S

APOLLAKE

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

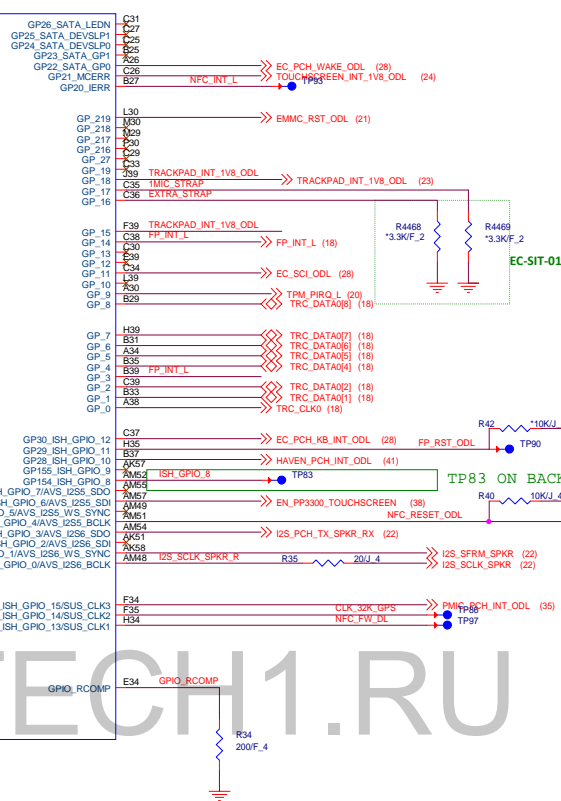
GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP

GPIO_RCOMP



6/23/16

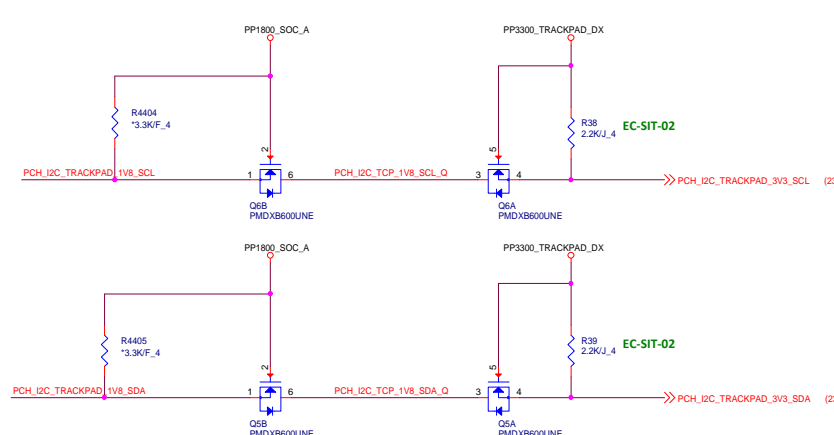
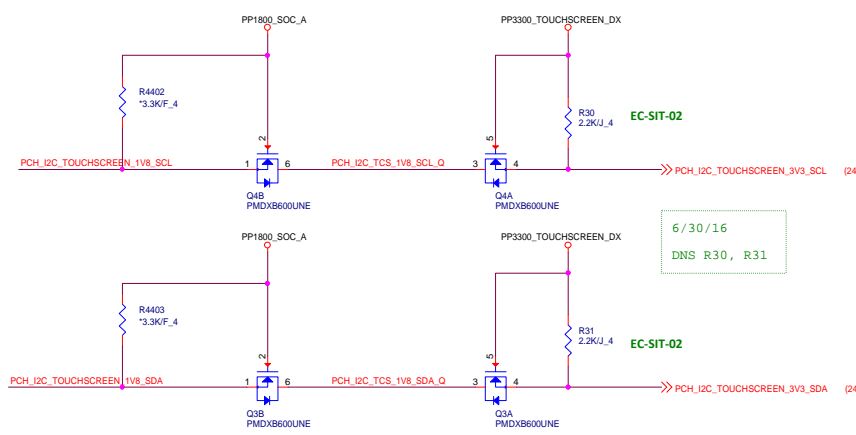
ADDED TRACKPAD_INT_1V8_ODL TO GP15
RENAMED TRC_DATA0[3] TO FP_INT_L

1MIC_STRAP	
0	4 MIC
1*	1 MIC

NFC GPIO

SPEAKER AMP

NFC GPIO



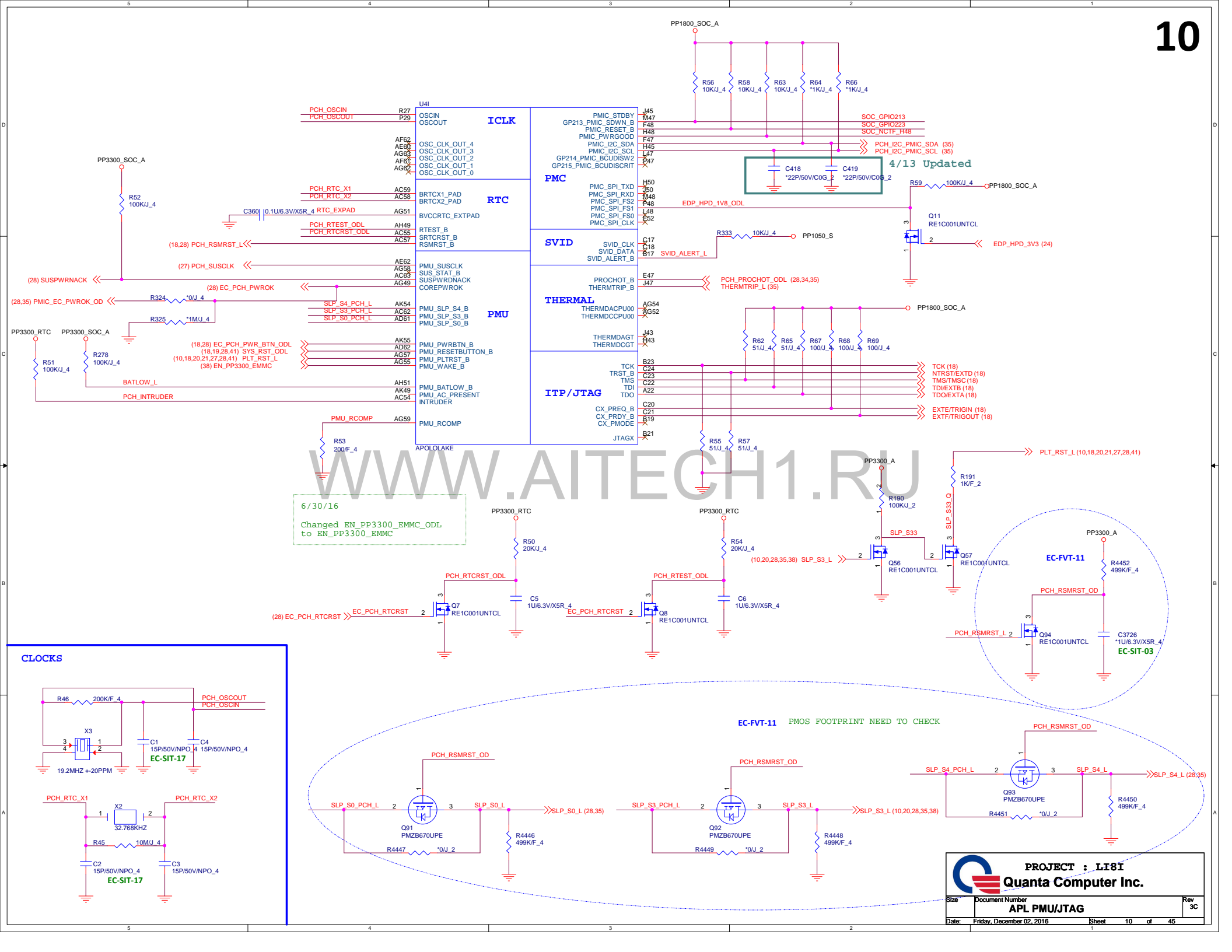
PROJECT : LI8I

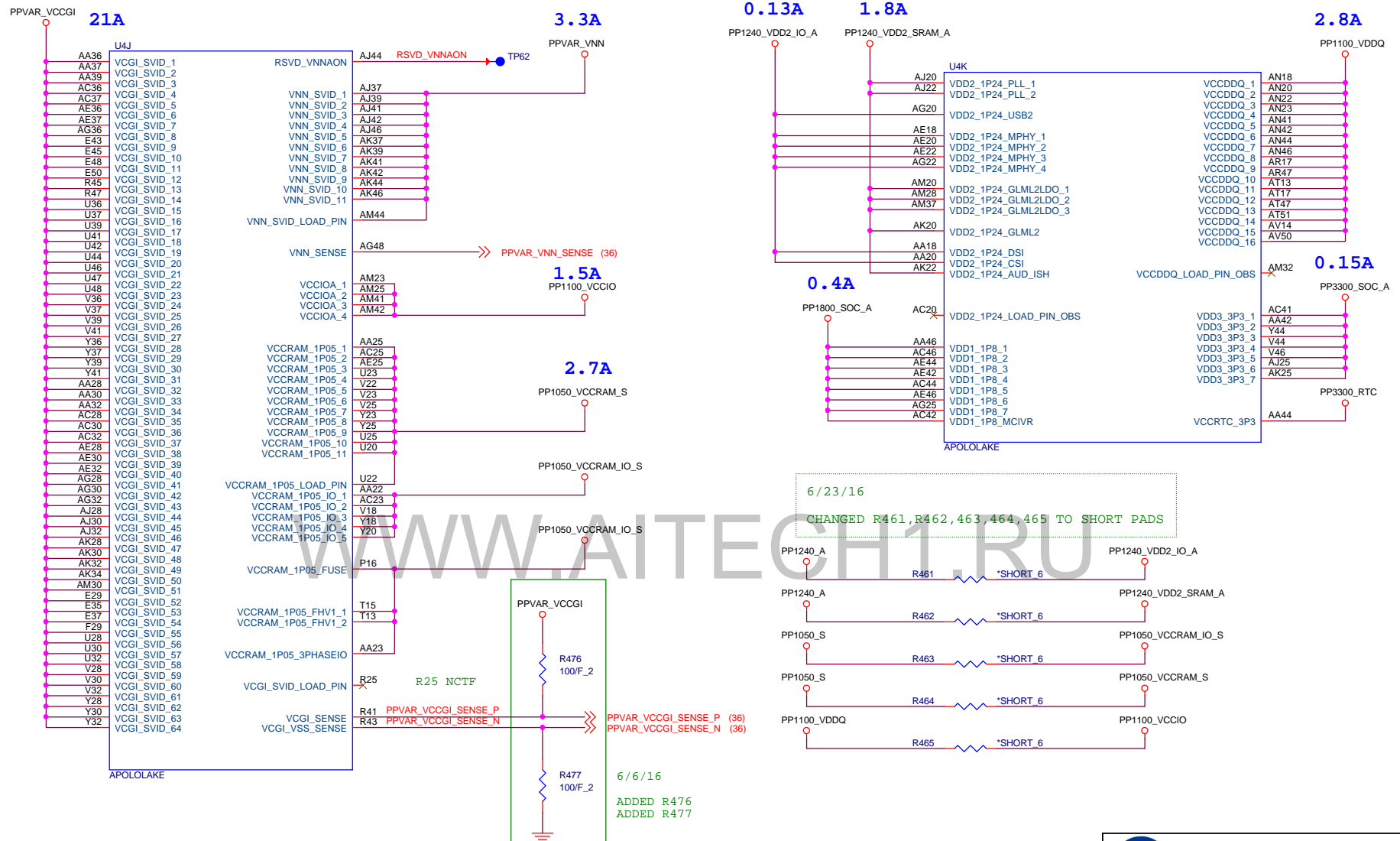
Quanta Computer Inc.

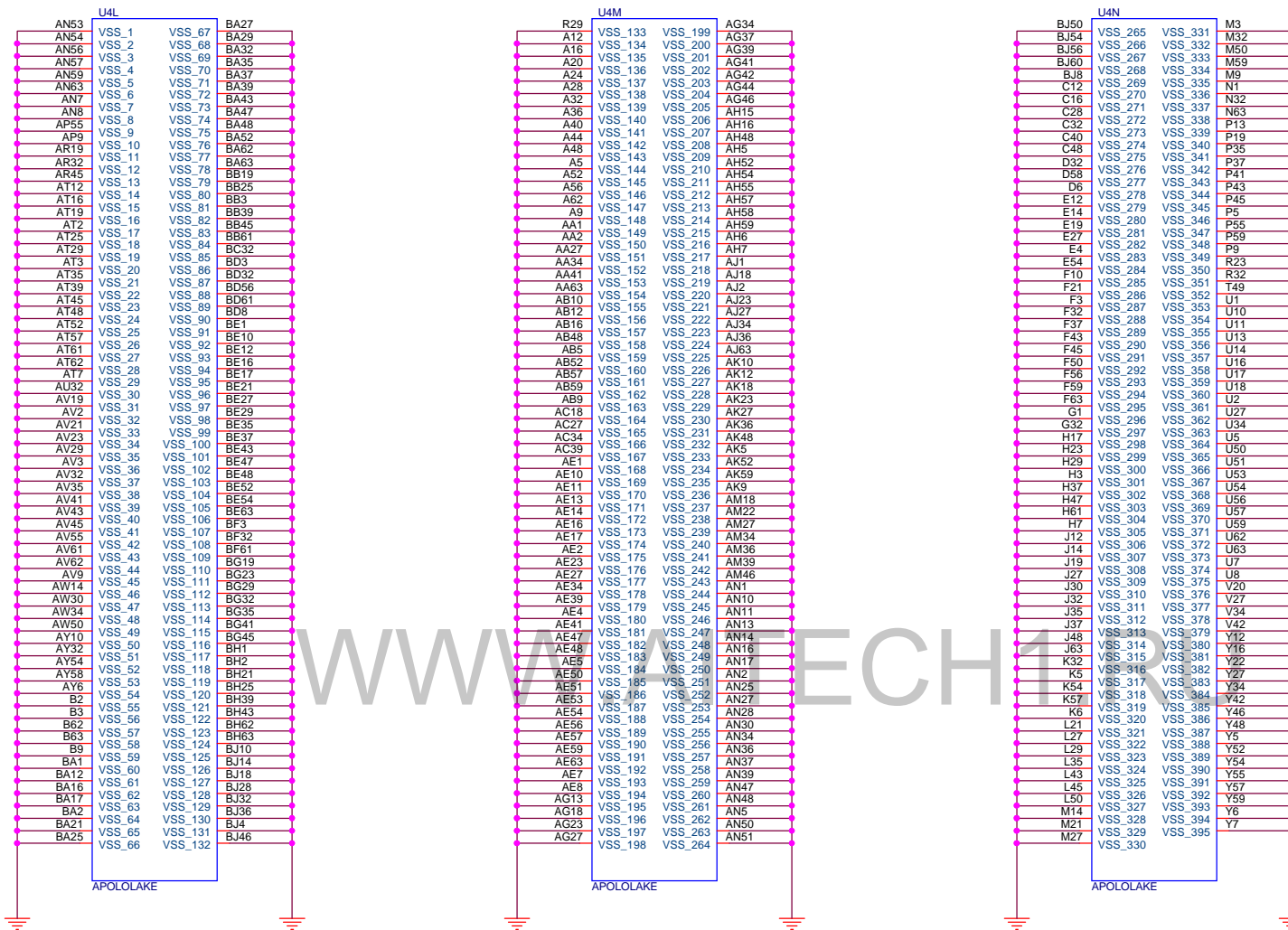
Size Document Number

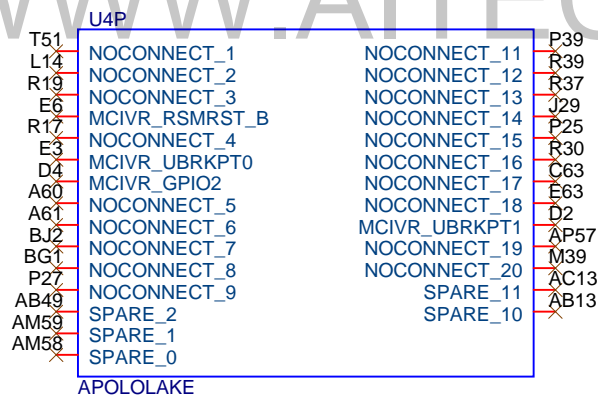
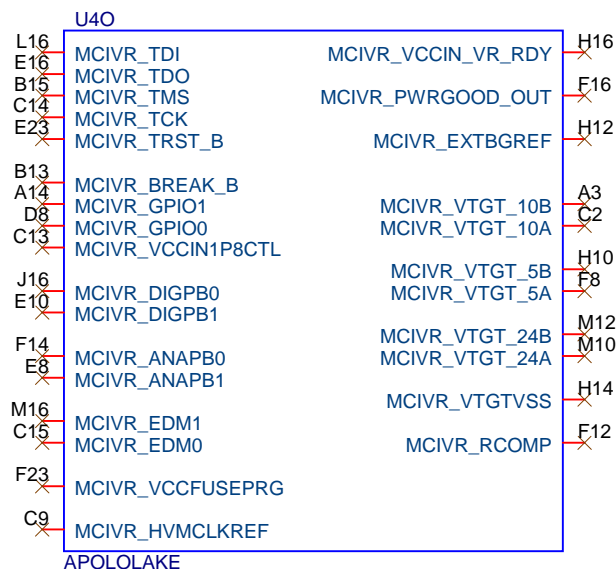
APL I2C/I2S/GPIO

Date: Monday, November 28, 2016 Sheet 9 of 45



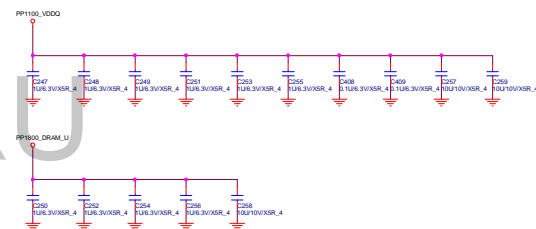
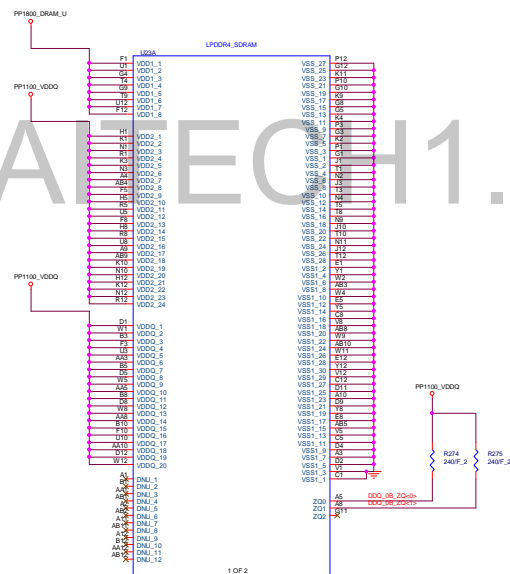
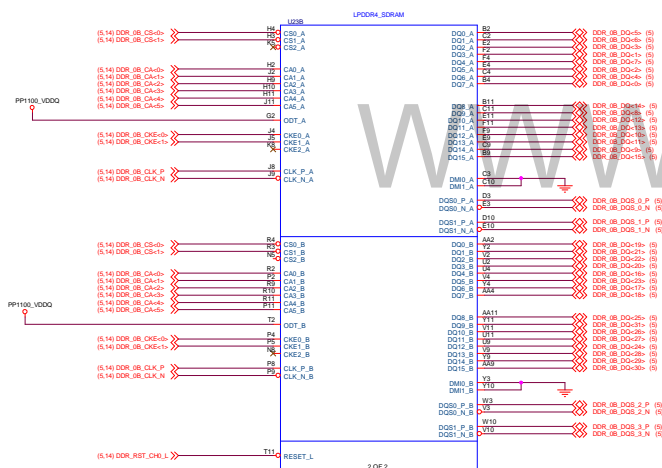
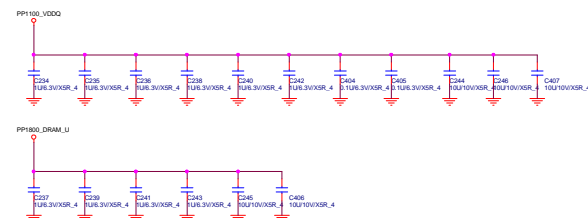
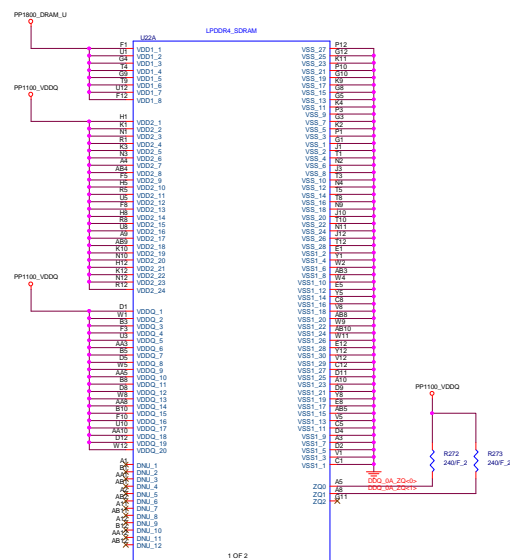
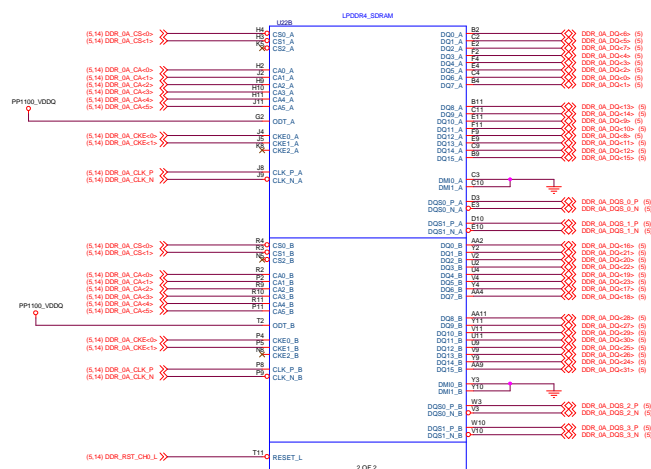


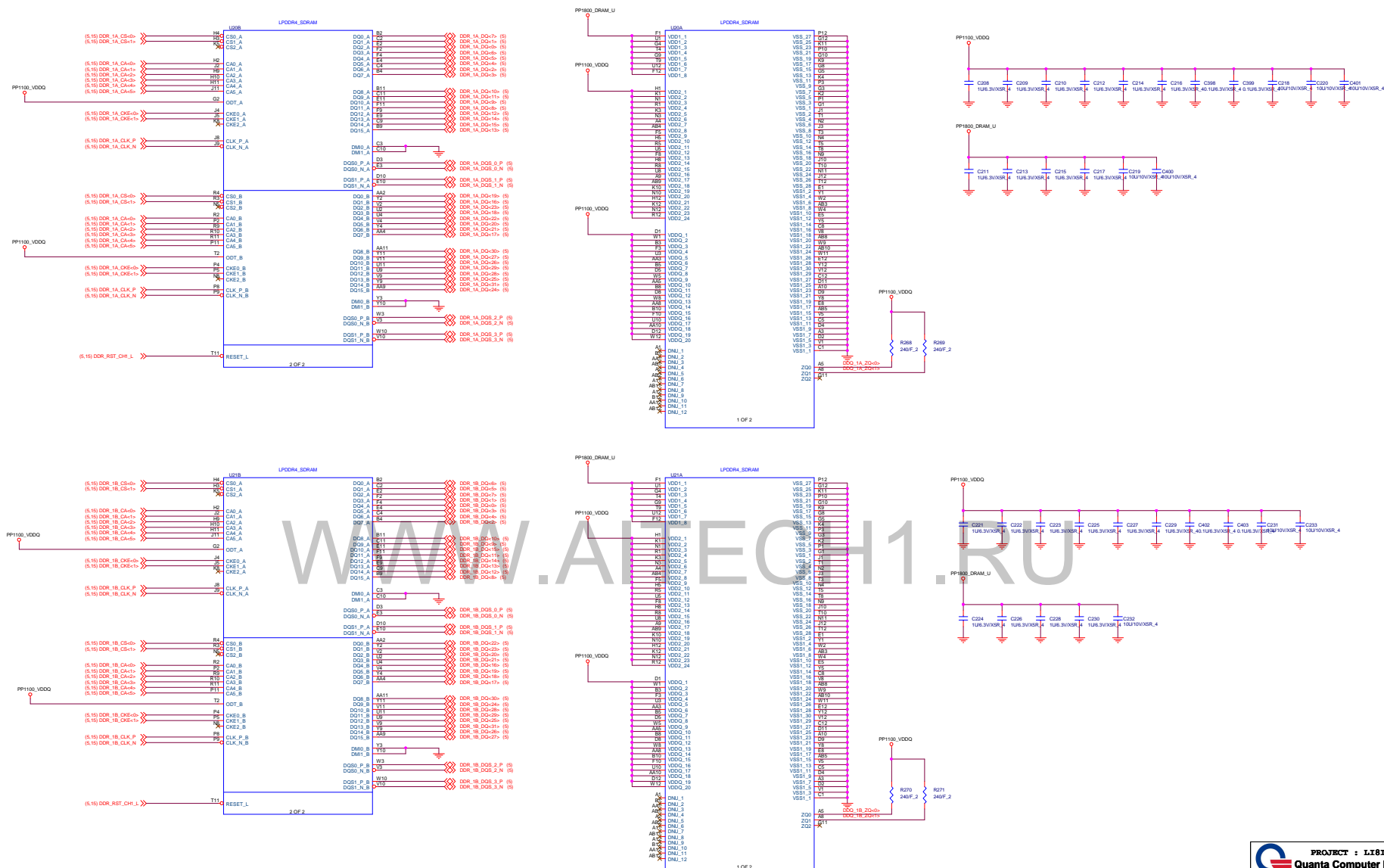


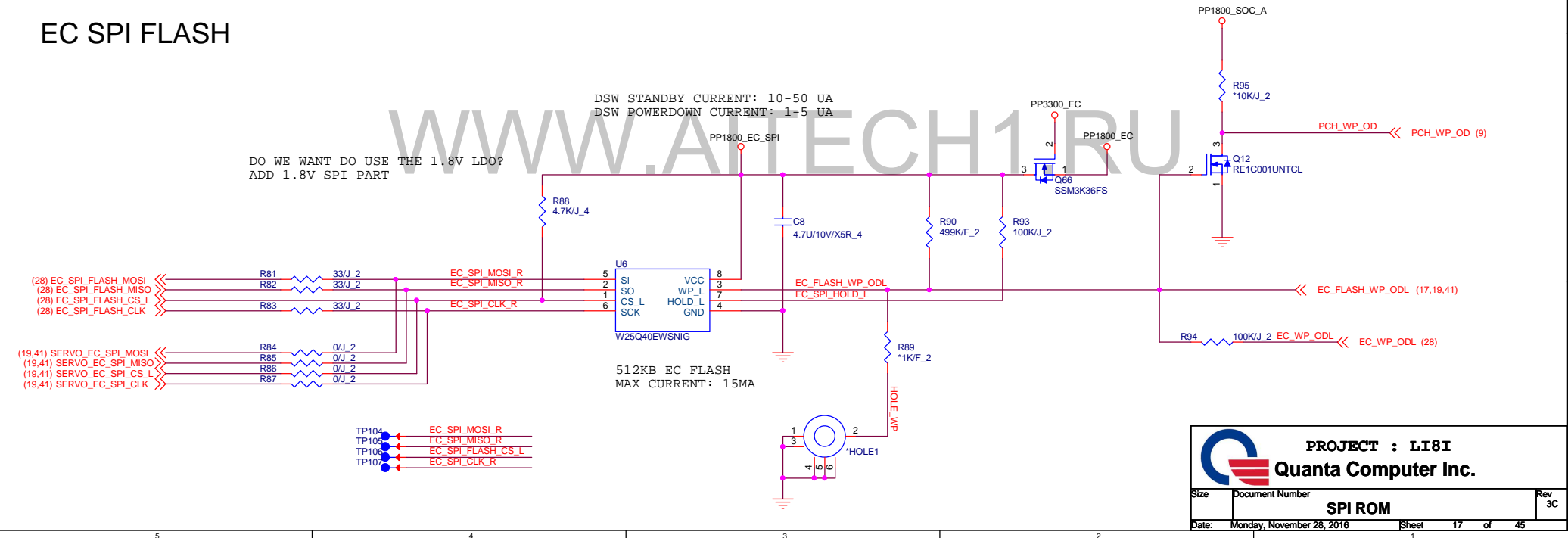


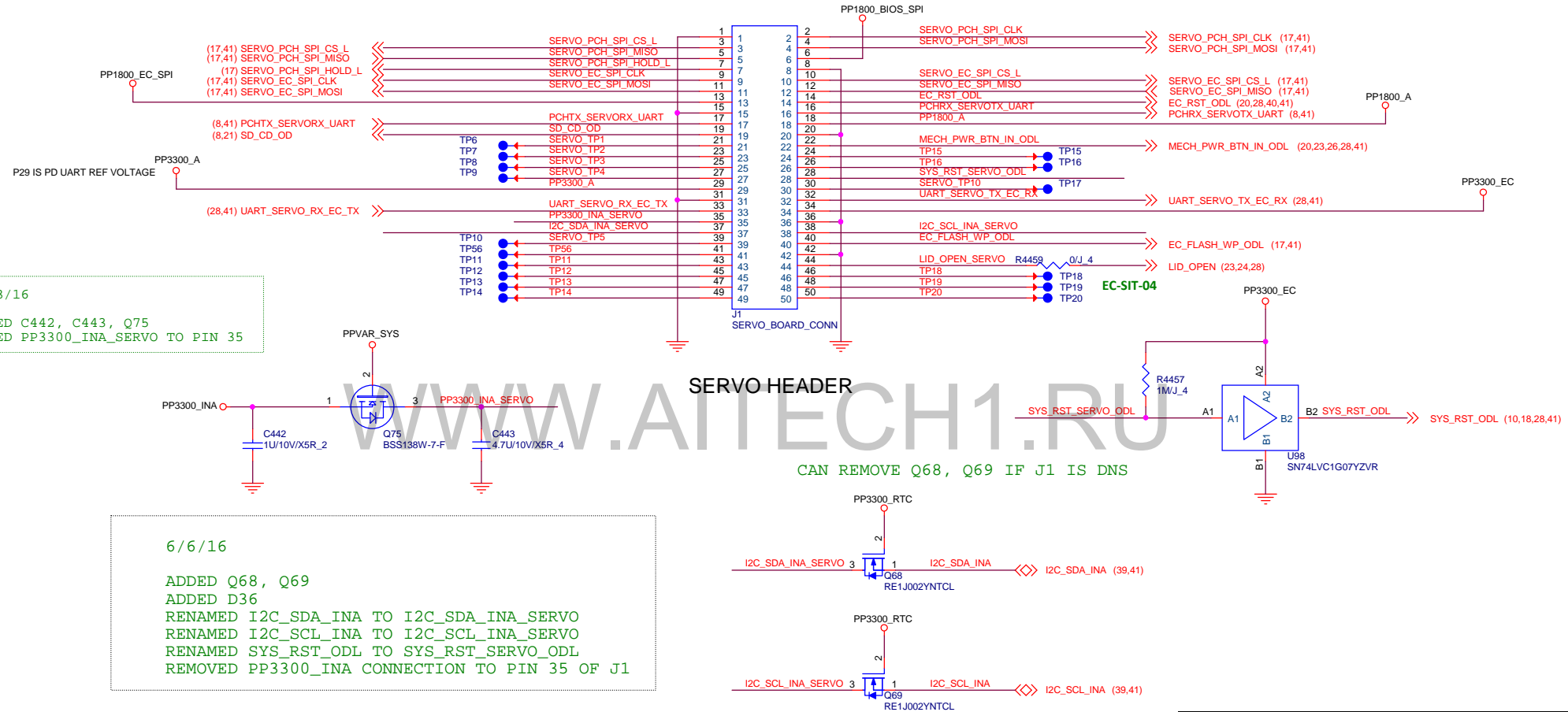
PROJECT : LI8I
Quanta Computer Inc.

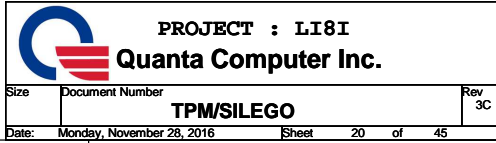
Size	Document Number	Rev
	APL NO CONNECT	3C
Date:	Monday, November 28, 2016	Sheet 13 of 45



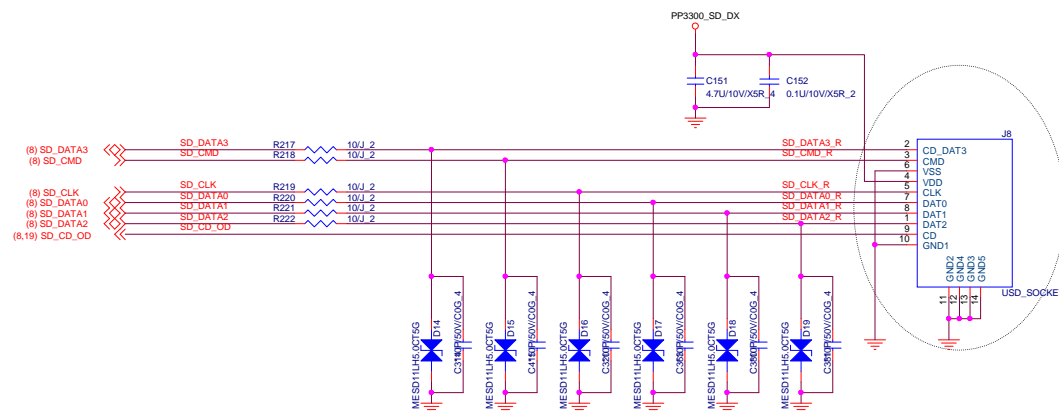
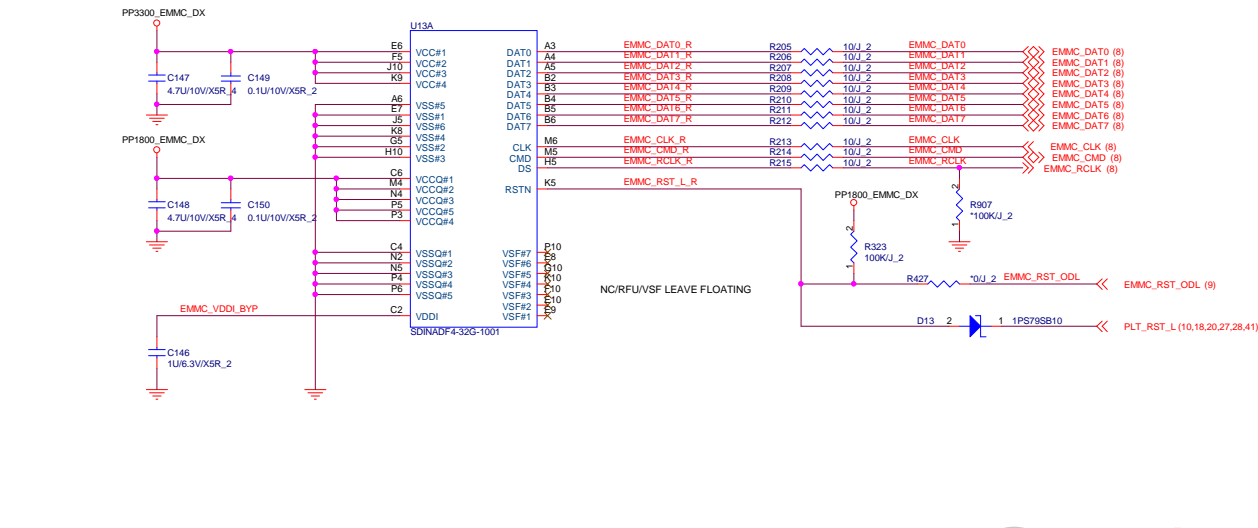




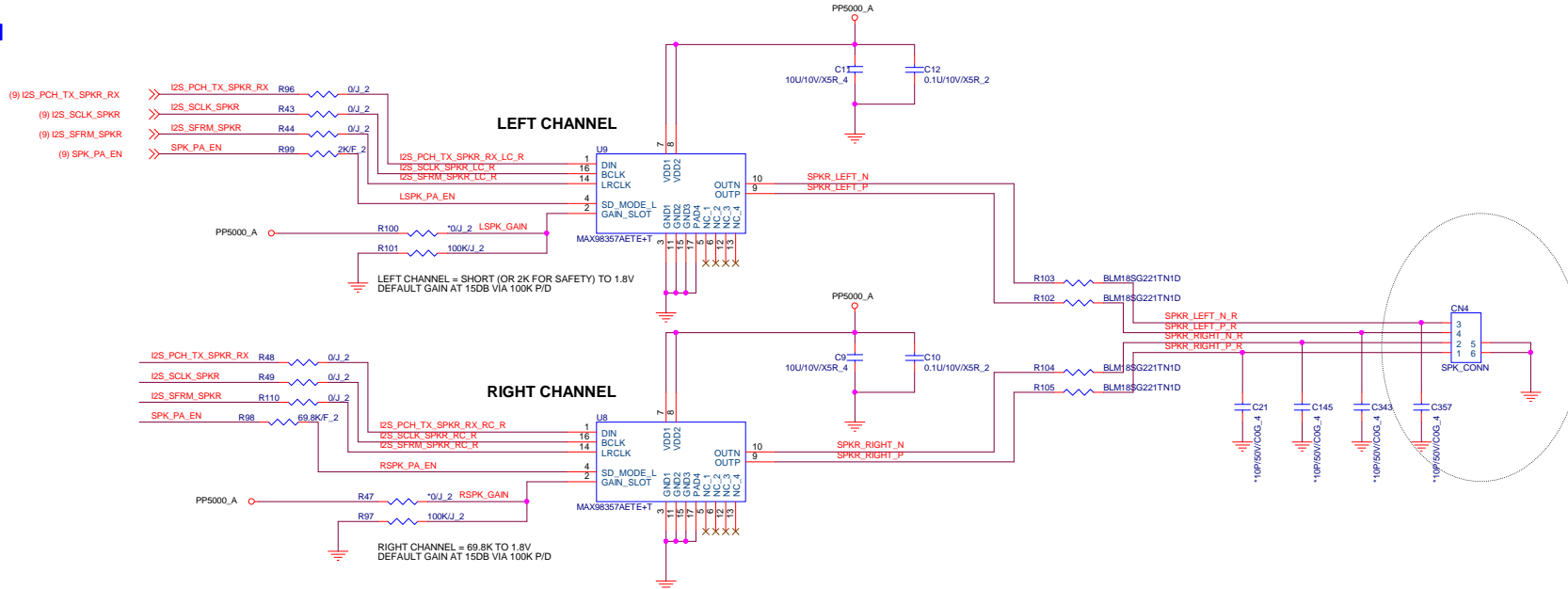




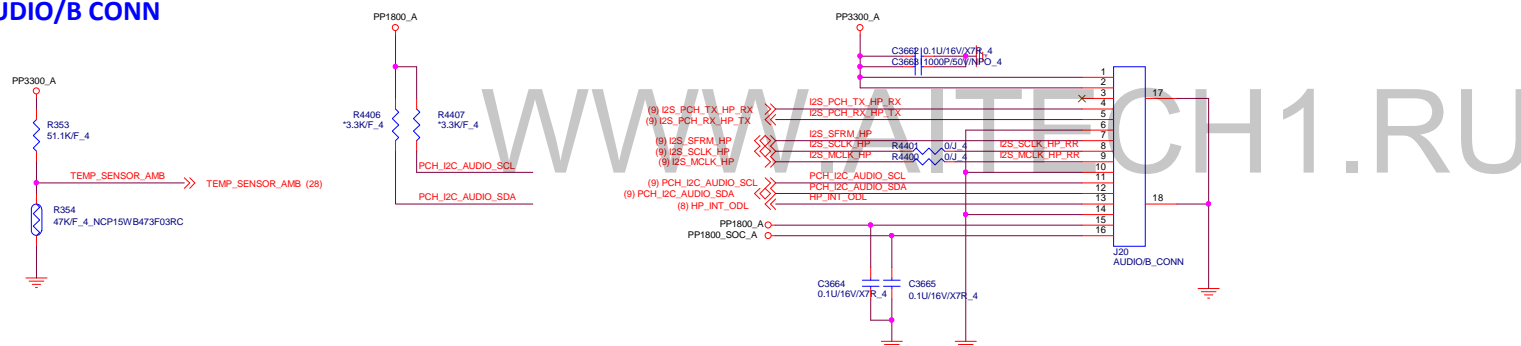
32 GB EMMC SD STORAGE




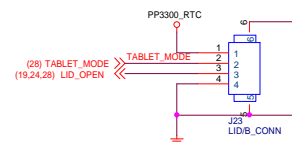
SPEAKER CONN



AUDIO/B CONN



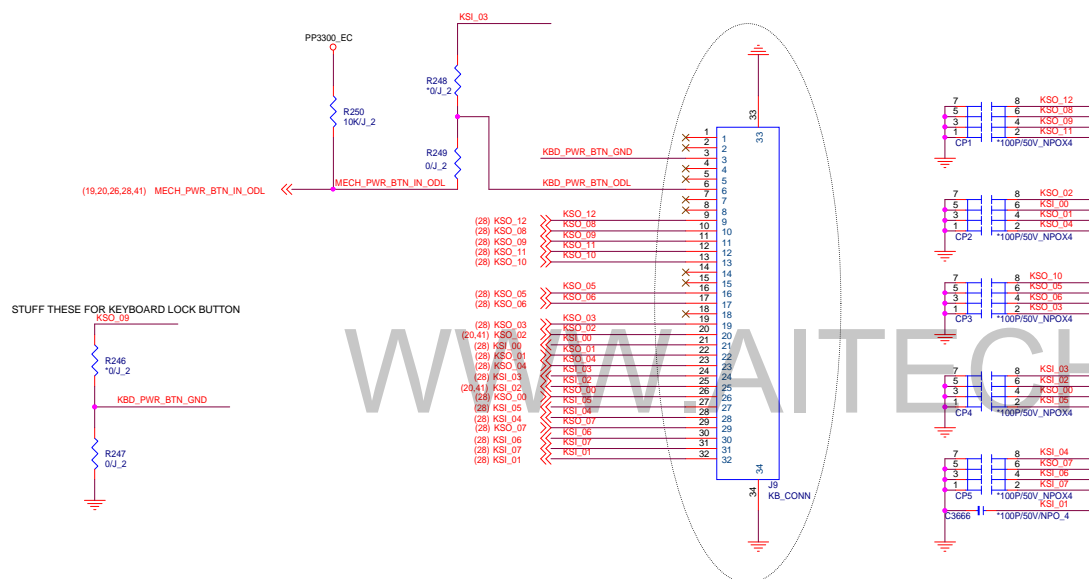
 PROJECT : LI8I Quanta Computer Inc.		
Size	Document Number	Rev
	AUDIO	3C
Date:	Monday, November 28, 2016	Sheet 22 of 45



7/25 remove Reef FP CONN

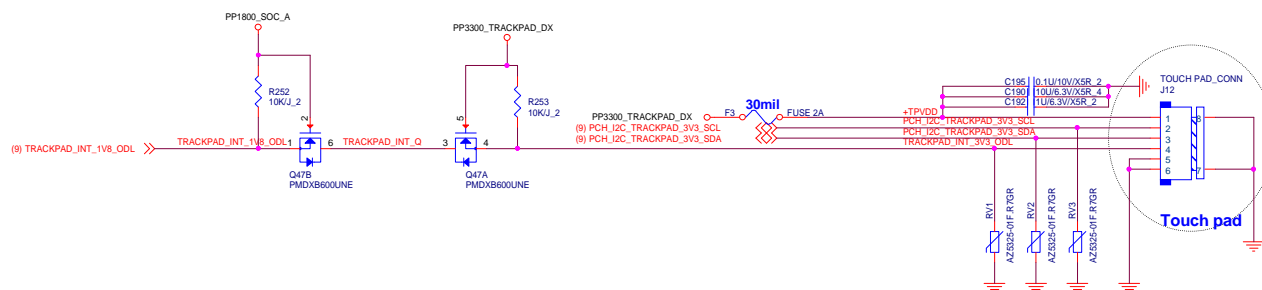
7/25 remove Reef NFC CONN

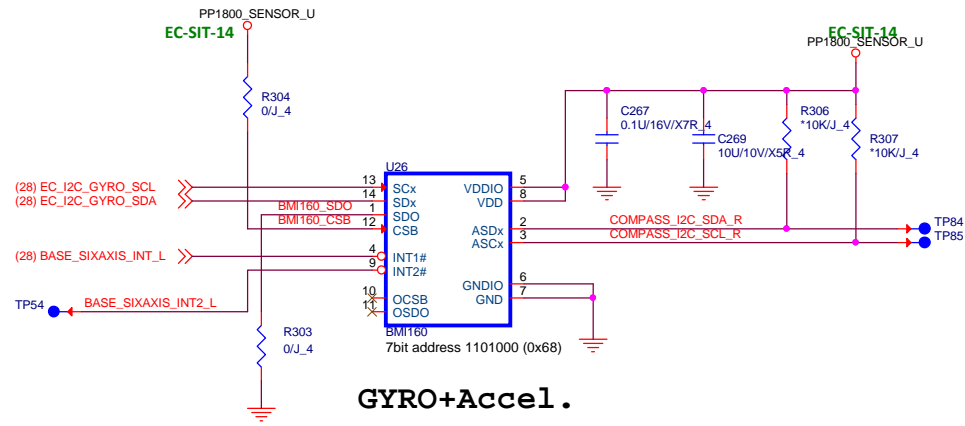
Keyboard CONNECTOR



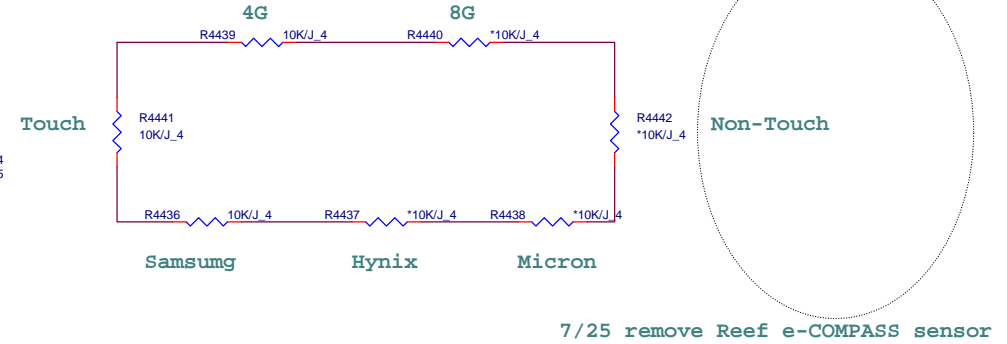
TRACKPAD CONNECTOR

SUBJECT TO CHANGE PER QUANTA REQUEST
TRACKPAD 3.3V TO 1.8V LEAKAGE SHOULD BE TINY






BOM control circuit put on BOT side

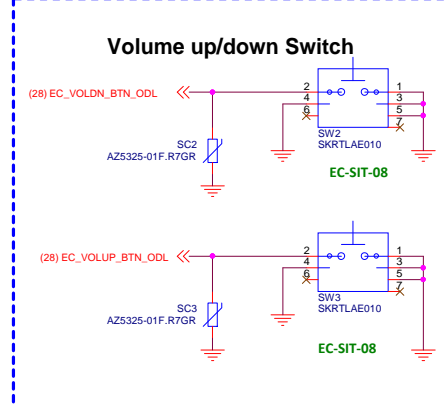
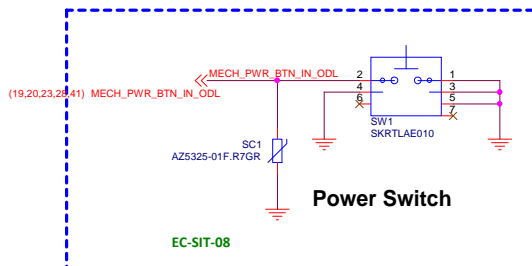


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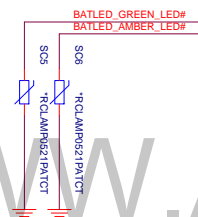
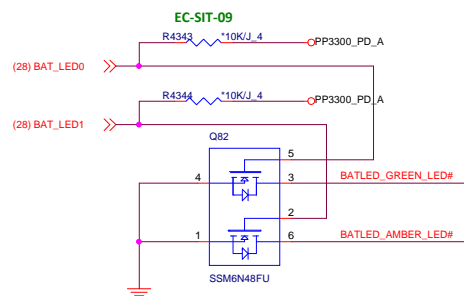
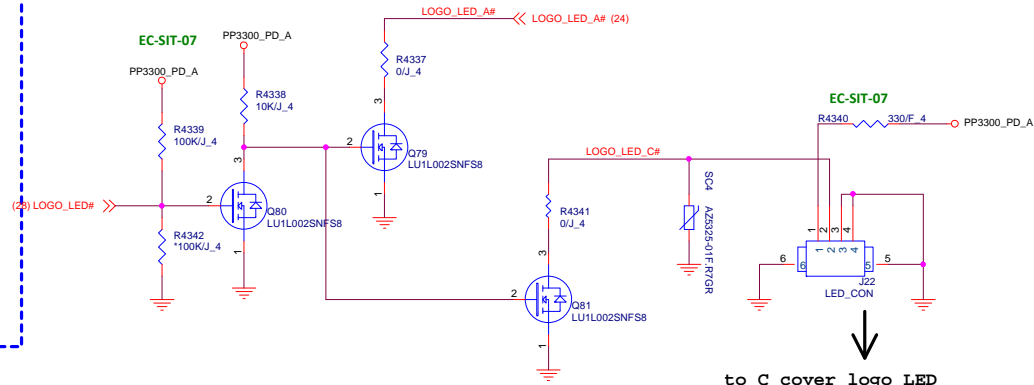
7/25 remove Reef Battery Charger LED circuit

7/25 remove Reef BAROMETER sensor

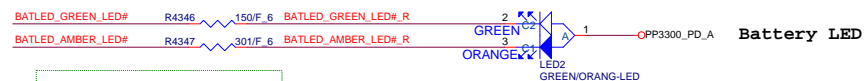
		PROJECT : LI8I	
		Quanta Computer Inc.	
Size	Document Number	COMPASS, BARO, GYRO, LID	
Date: Monday, November 28, 2016	Sheet 25 of 45	Rev 3C	




LED Driver



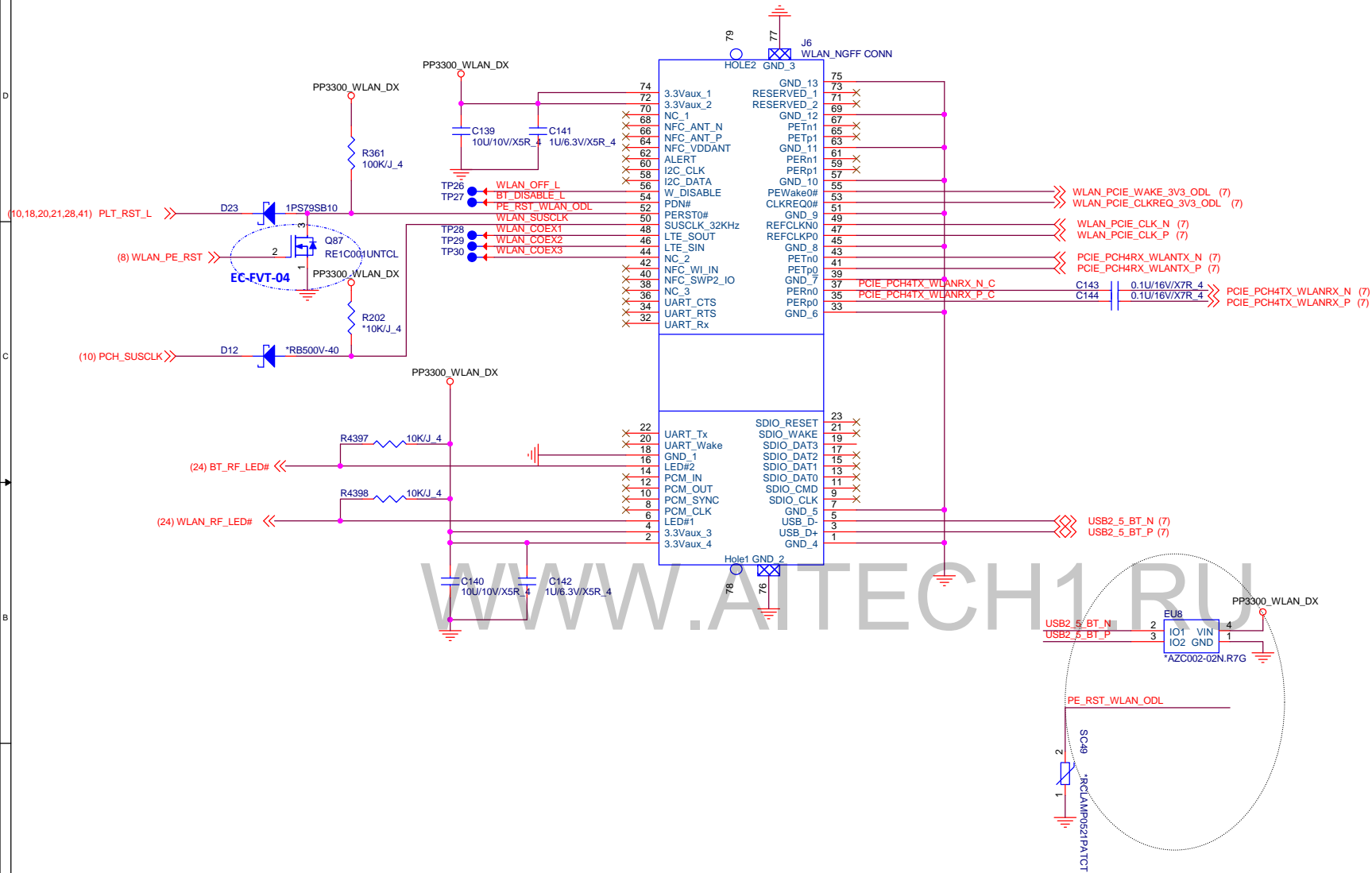
RESISTORS BASED ON 10MA
TUNE VALUES BASED ON LEDS
EC CAN DRIVE 12MA



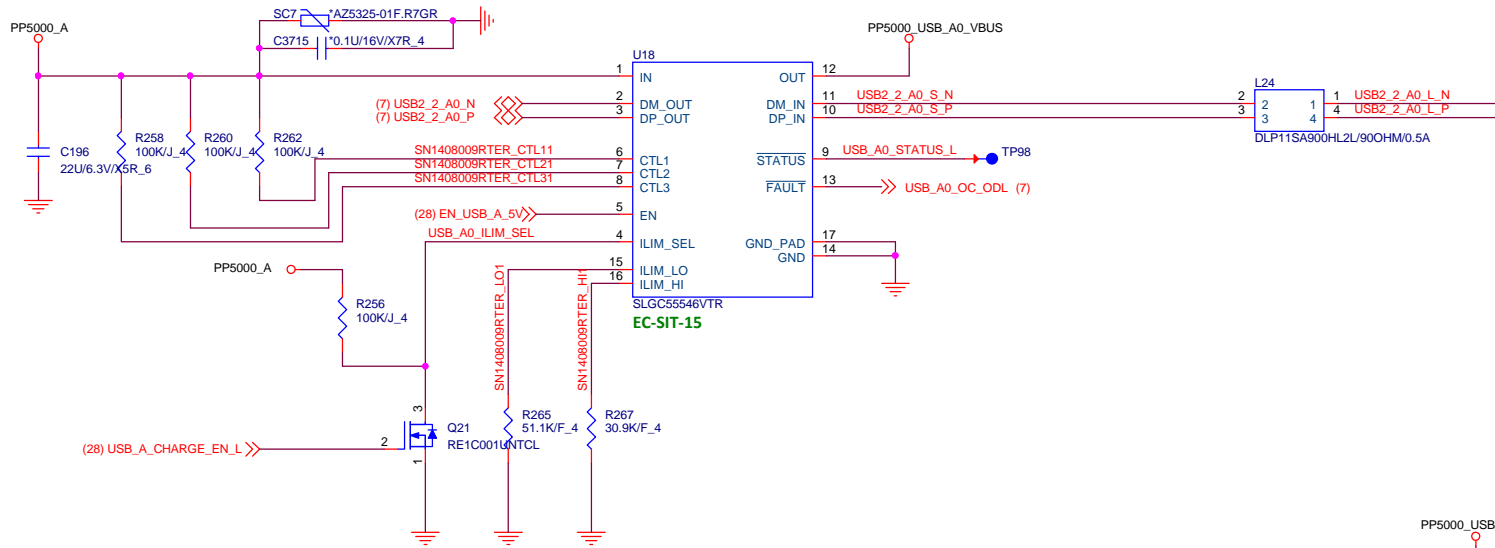
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		PROJECT : LI8I	
		Quanta Computer Inc.	
Size	Document Number	POWER BUTTON	
Custom			
Date:	Monday, November 28, 2016	Sheet	26 of 45
		Rev	3C

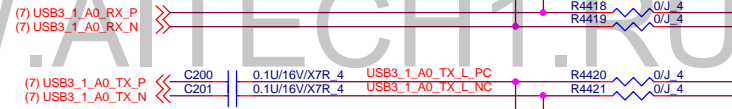
M.2 connector



7/25 remove Reef GPS CONN



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For ESD



PROJECT : LI8I

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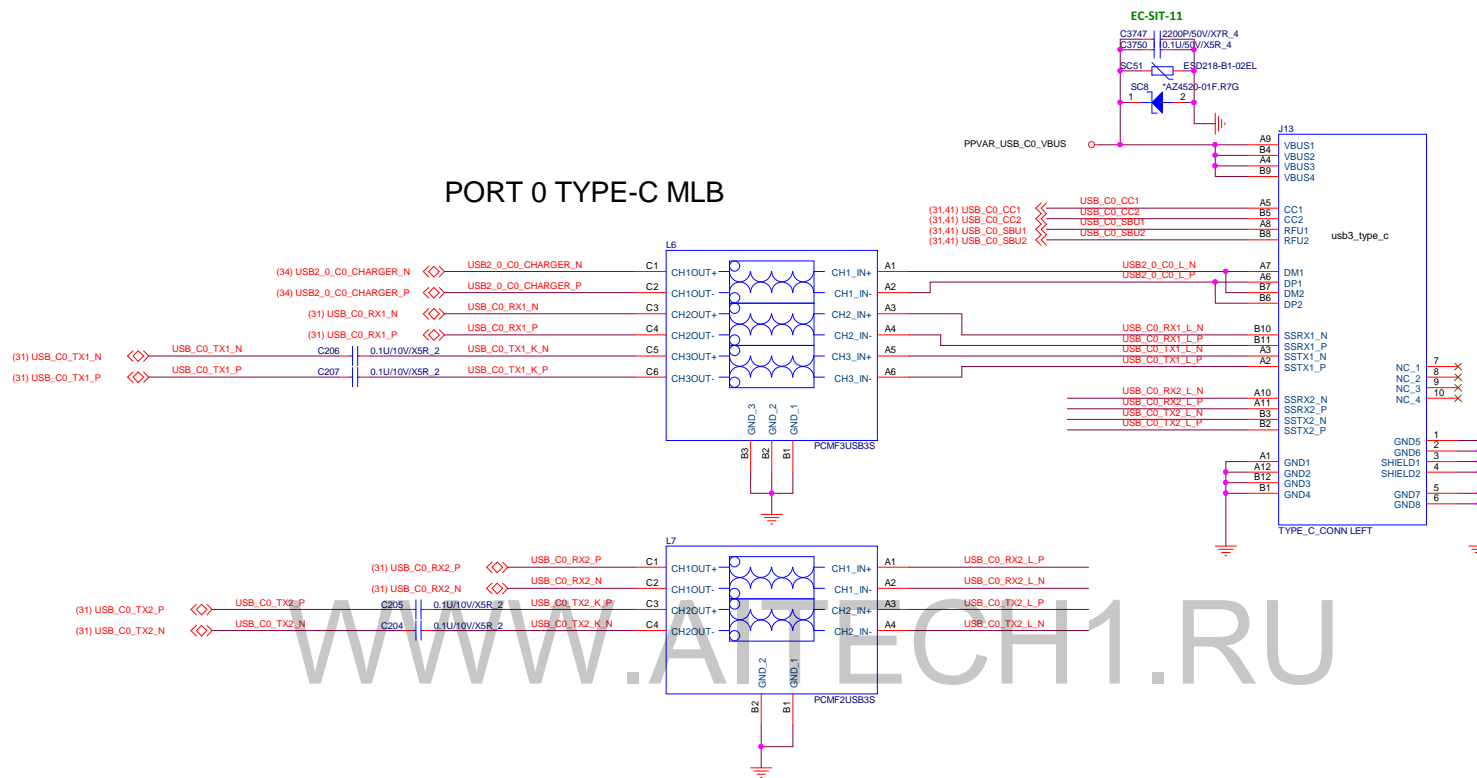
Size Document Number

USB A CONNECTORS

Date: Monday, November 28, 2016 Sheet 29 of 45

Rev 3C

PORT 0 TYPE-C MLB

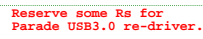


8/15 reserve for ESD



6/6/16

RENAME USB PD RST ODL TO USB C0 PD RST ODL



EC-SIT-1

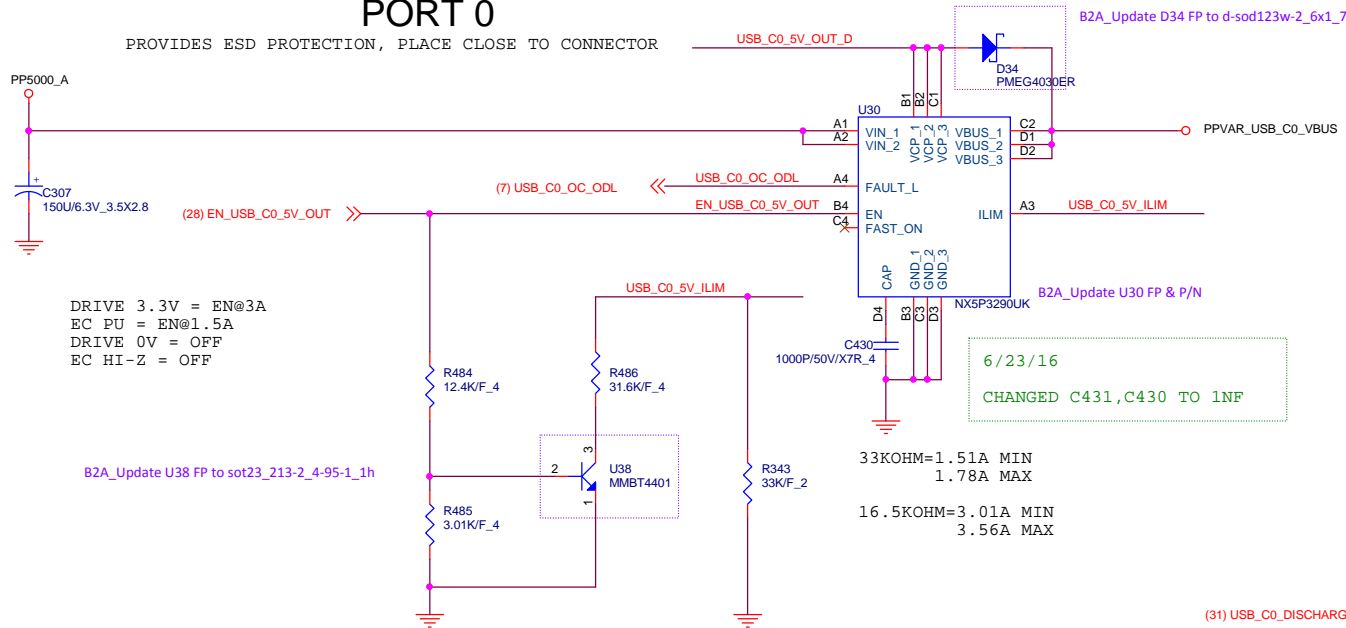
Debug

0/J_4B_DE



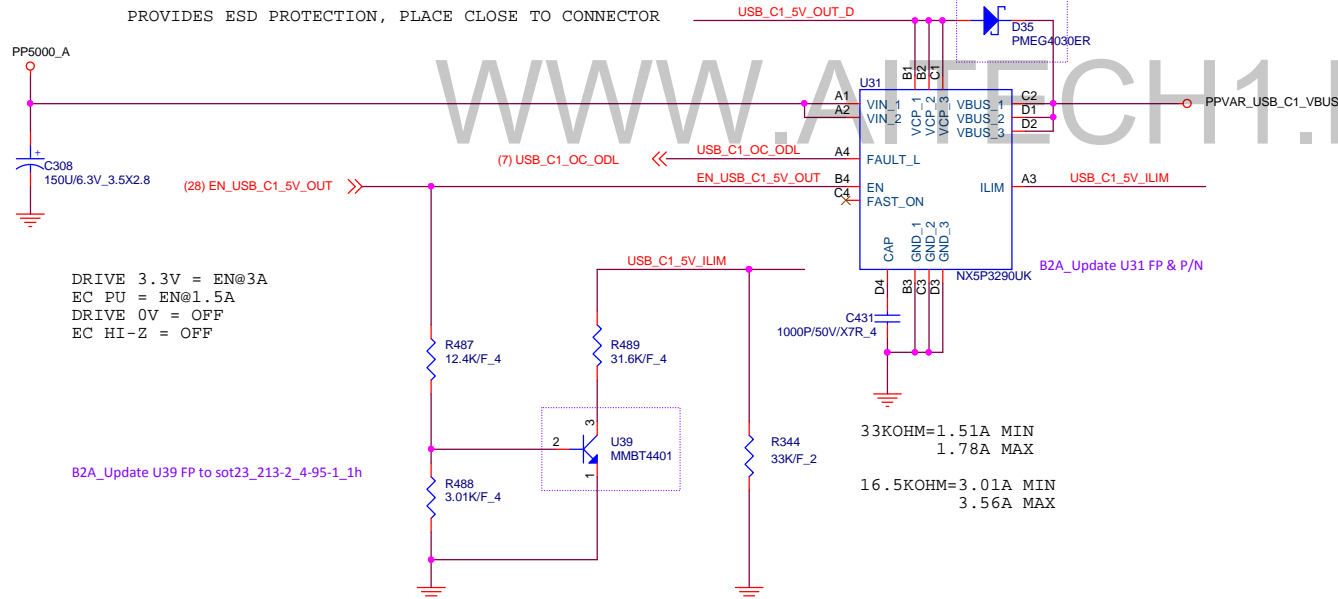
PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



PORT 1

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



```

20UF LOAD, 21V TO <0.8V IN <80MS
20UF LOAD, 5V TO <0.8V IN <45MS
0402 CAN DISSIPATE 400MW FOR 80MS
0603 CAN DISSIPATE 400MW FOR 500MS
0805 CAN DISSIPATE 400MW FOR 2000MS

```

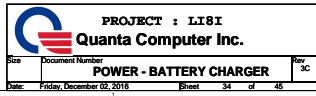


PROJECT : LI8I
Quanta Computer Inc.

Size	Document Number	Rev
	USB C 5V OUT	3C
Date:	Monday, November 28, 2016	Sheet 33 of 45

6/30/16

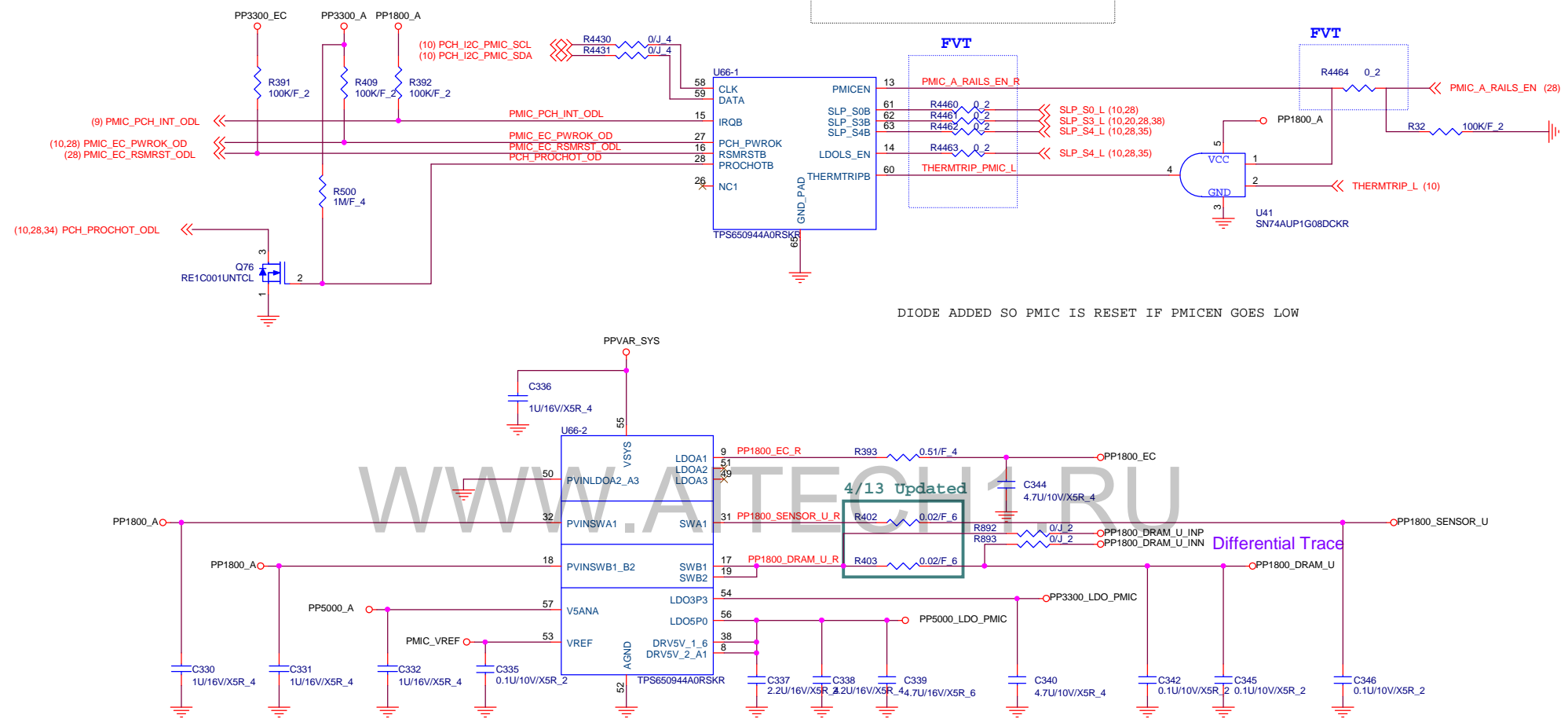
CHANGED R328,R330 to short pads

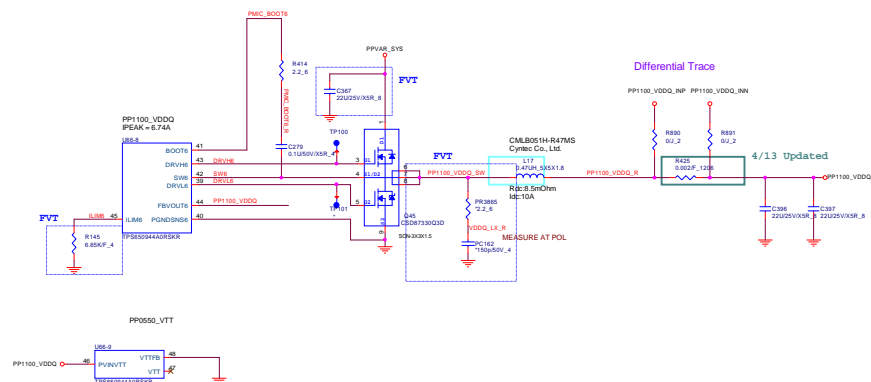


POWER - PMIC LOGIC

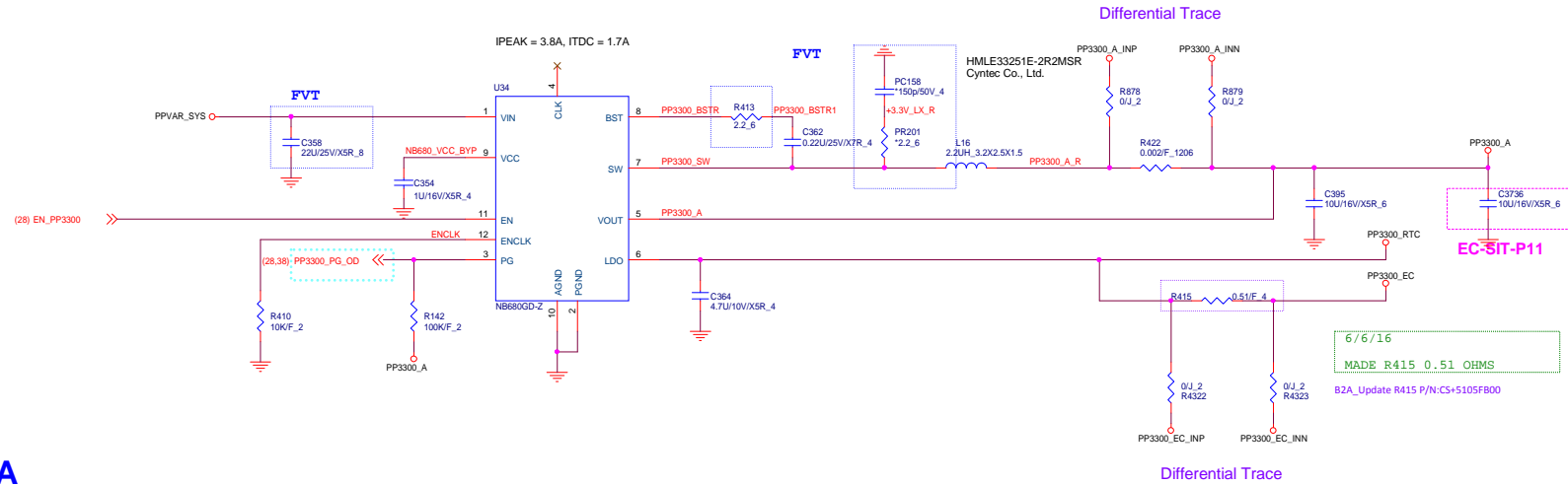
35

6/6/16
STUFFED D2
ADDED R475
CHANGED R32 TO 51K
ADDED D33

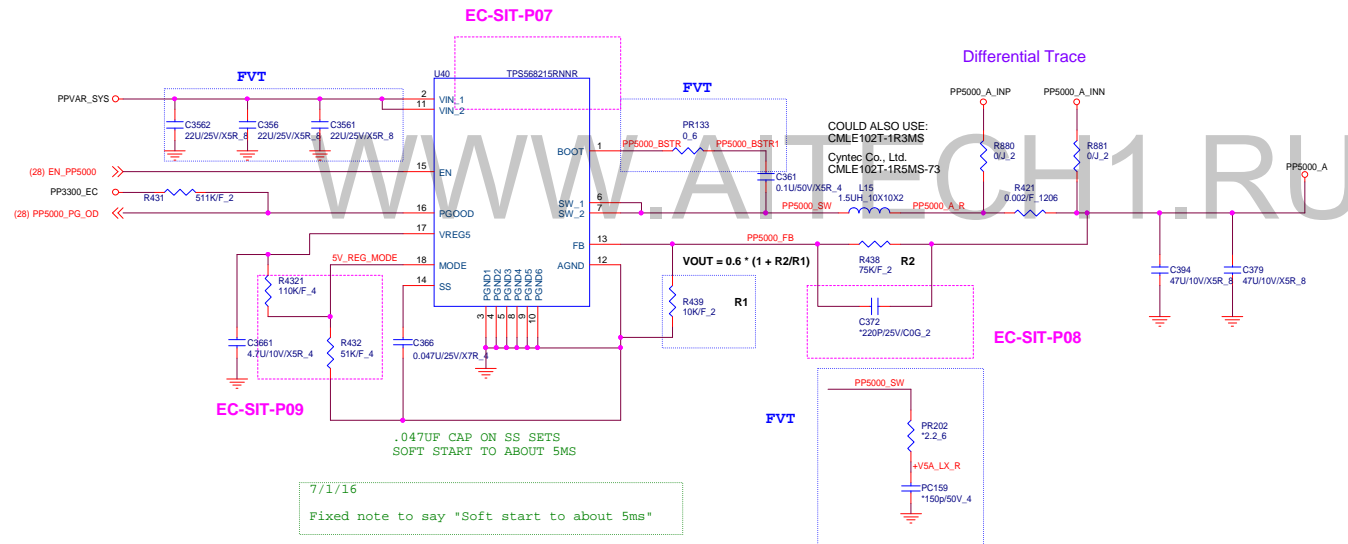




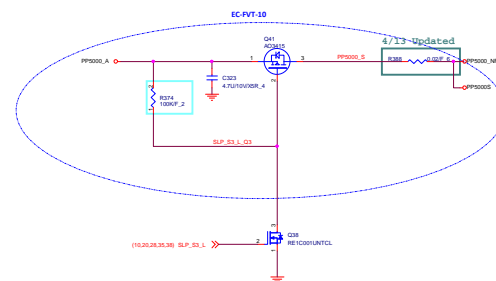
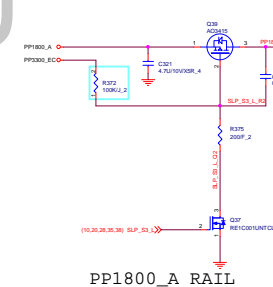
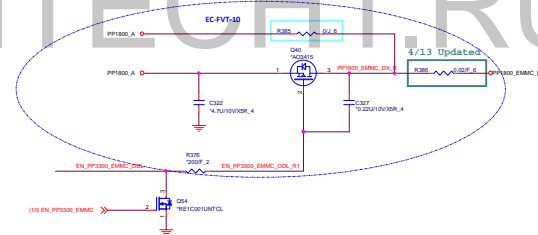
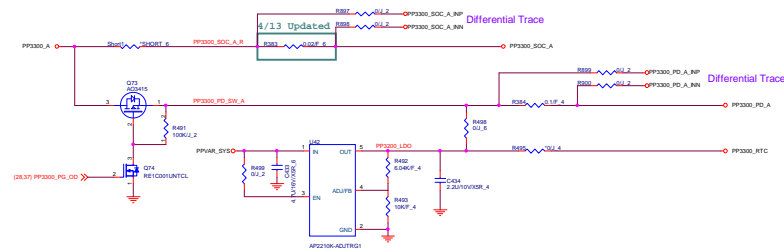
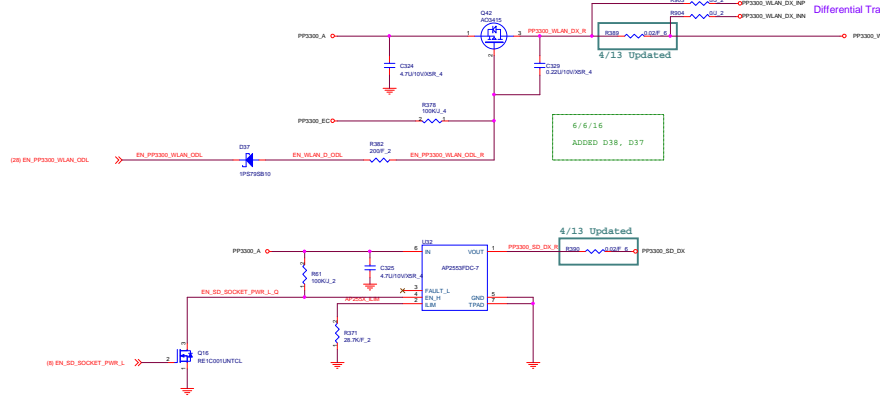
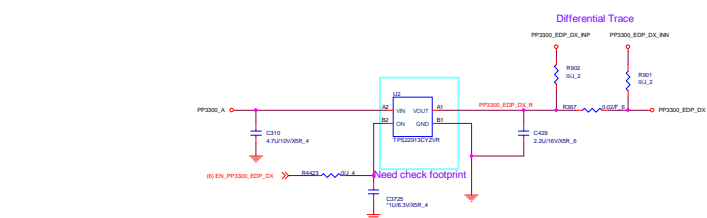
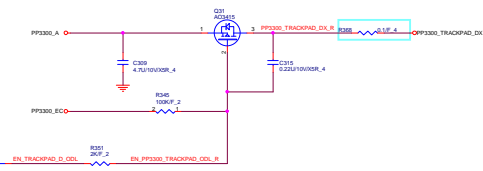
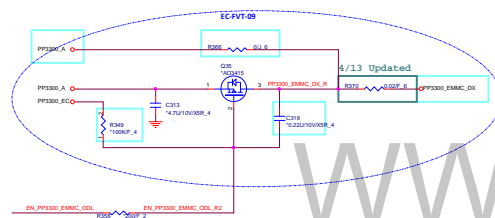
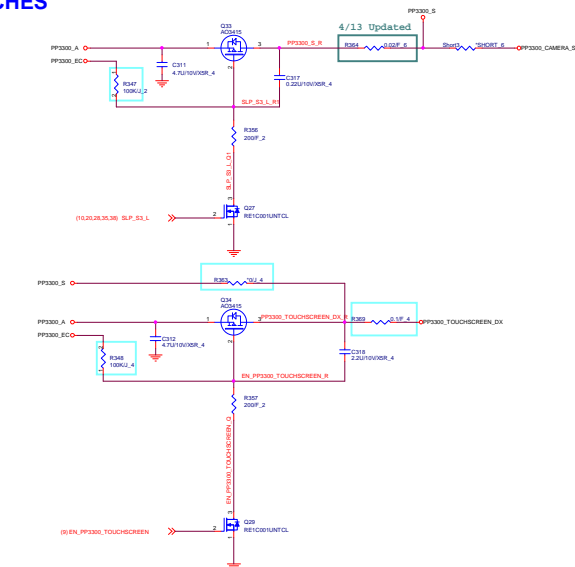
PP3300_A



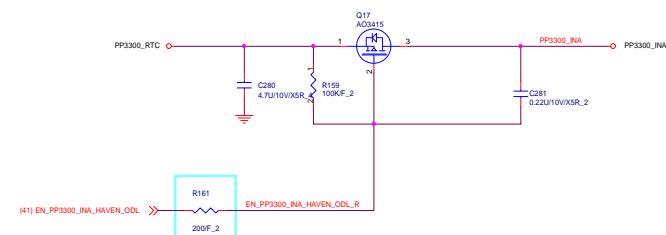
PP5000_A



POWER - LOAD SWITCHES

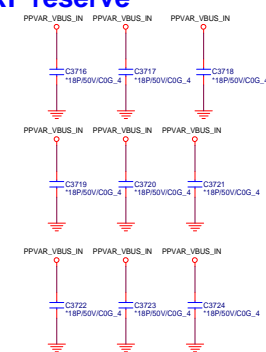


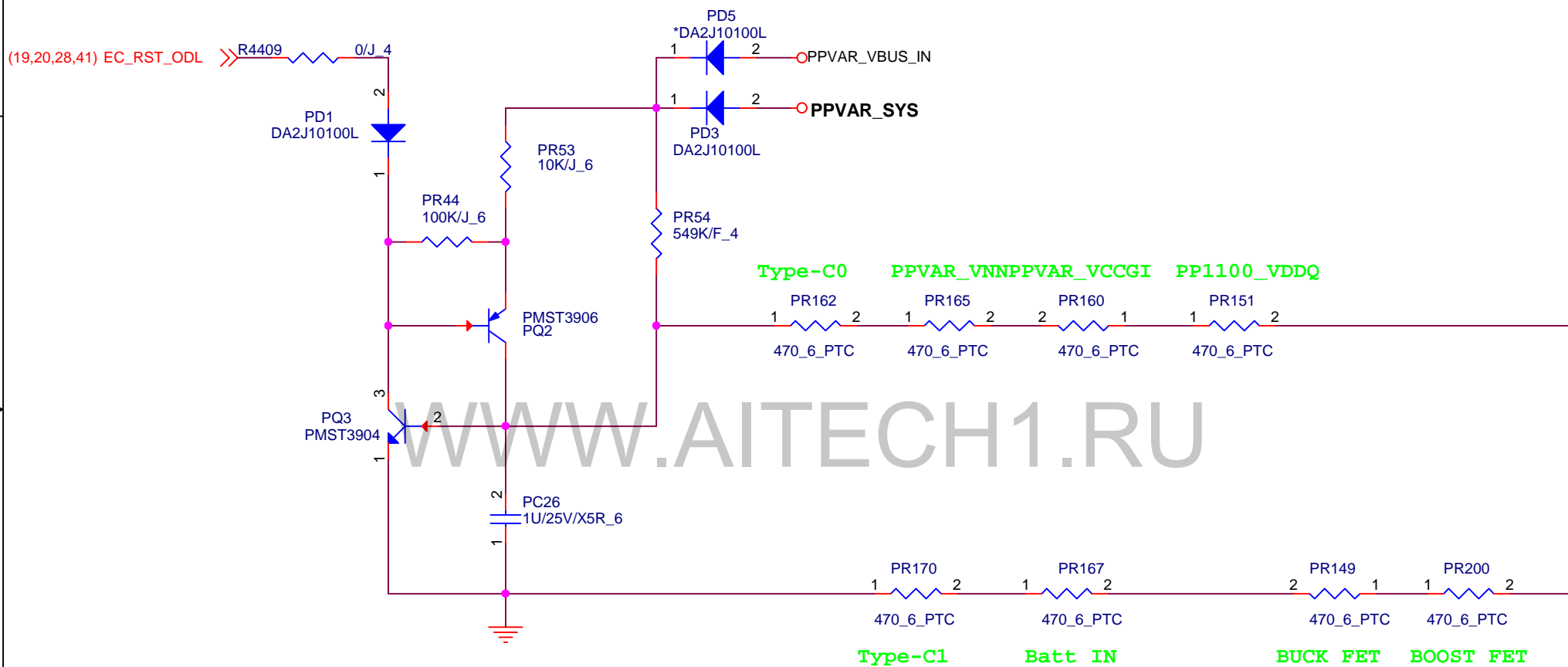
PP5000_A RAIL



POWER TEST PAD

RF reserve



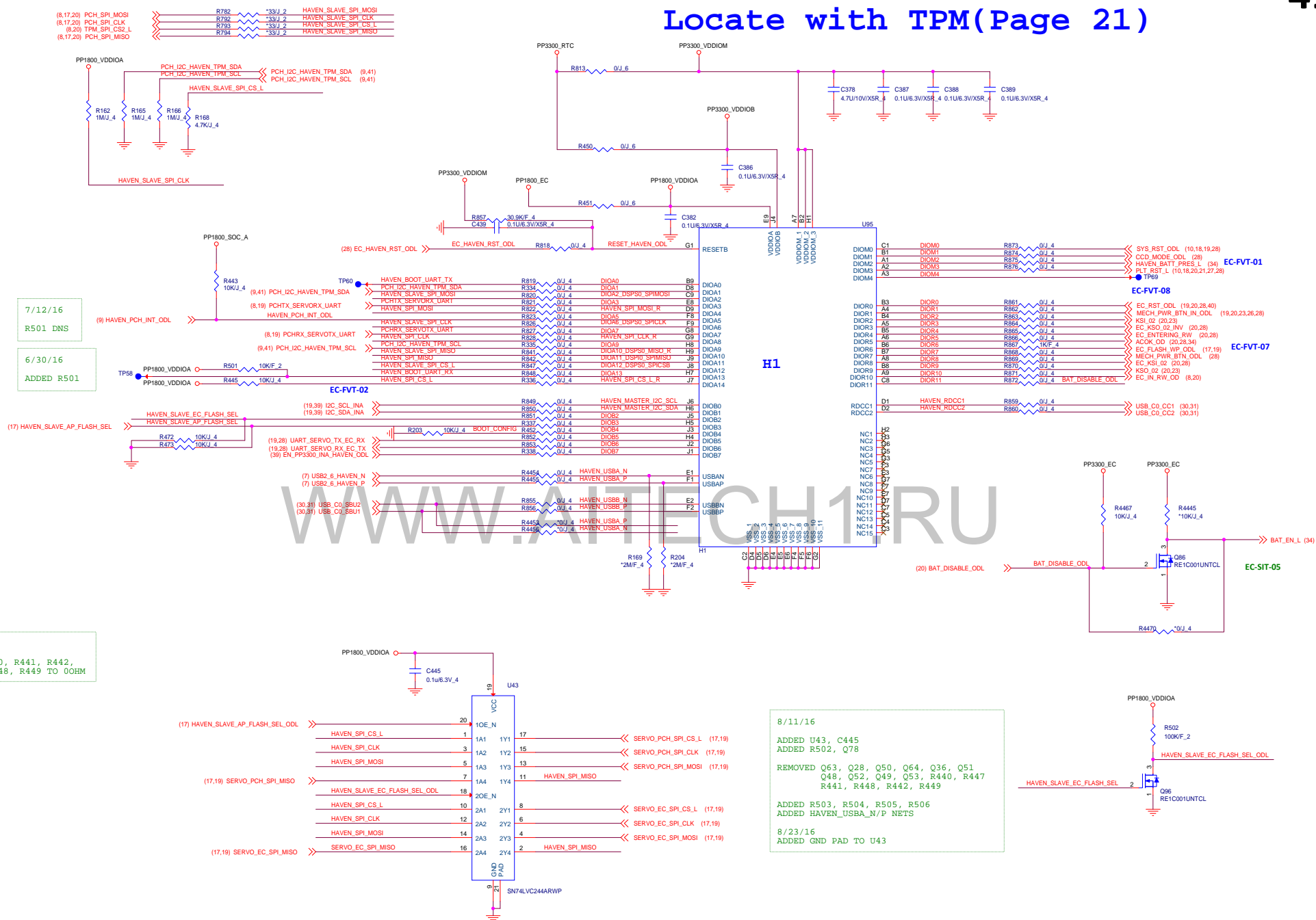


PROJECT : LI8I
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Size	Document Number	Rev 3C
Date: Monday, November 28, 2016	Sheet 40 of 45	

PTC Circuit

Locate with TPM(Page 21)



C. The soft-start implementation was preventing the if	Removed C328, R337 Pulled R374 to PP5000_A
---	---

LI8I/J EE Schematic EC Tracking Record B to C version(FVT to SIT Planar)

EC #	Page	Description	Part Affected
EC-SIT-01	09	Added MIC_STRAP table for strapping option for 1 or 4 mics	reserve pull down circuit and connect to GP_16/GP17 with R4468/R4469
EC-SIT-02	09	Change R30/R31/R38/R39 value from 1.8k to 2.2k for adjusting I2C CLK frequency under 400KHz	Change R30/R31/R38/R39 BOM to 1.8K
EC-SIT-03	10	This makes the rise time too long and keeps the switches on all the time	DNS C3726
EC-SIT-04	19	Change R4450 to 0 ohm for following reference board design	Change R4459 to 0 ohm
EC-SIT-05	20 41	Following reference board design: 1.Change net name from BAT_EN_L to BAT_DISABLE_ODL of Q46 circuit 2.Change R4467/R4445 pull high power rail from PP3300_RTC to PP3300_EC 3.Reserve R4470	Q46/R4467/R4445/R4470
EC-SIT-06	24	Reduce S3 leakage: Remodify RF LED control circuit	Remove D41 and add D43/D44
EC-SIT-07	24 26	Logo LED behavior error and remodify logo LED control circuit 1.Change power rail from PP5000_A to PP3300_PD_A 2.Change R4432/R4340 BOM to 330 ohm 3.Change R4339/R4338 power rail from PP5000_A to PP3300_PD_A	R4332/R4340/R4339/R4338
EC-SIT-08	26	ME change switch button design	Change SW1/SW2/SW3 bom to DHPSKRTLA00
EC-SIT-09	26	DNS R4343/R4344 due to internal pull high of EC GPIOs	DNS R4343/R4344
EC-SIT-10	28	Follow Google reference board board ID	change R37 BOM to 32.4K
EC-SIT-11	30	EMC recommend to reduce EMI noise and ESD protection 1.Add C3747/C3750/SC51/C3749/C3751/SC52 2.DNS SC8/SC23	1.Add C3747/C3750/SC51/C3749/C3751/SC52 2.DNS SC8/SC23
EC-SIT-12	31	For USB3.0 signal quality and remove USB3.0 co-lay circuit	Remove R4426/R4424/R4425/R4427/R4352/R4353/R4354/R4355
EC-SIT-13	32	Change USB2_1_C1_CHARGER common mode choke to DLP11SA900HL2L/90OHM/0.5A	L22/L25
EC-SIT-14	25 28	Follow Google reference board and change power rail of gyro to PP1800_SENSOR_U	R304/R306/R307/C267/C269R137/R135/U26
EC-SIT-15	29	Needed to fix 5V load switch issues where CDP is lost	Changed U18 BOM to SLGC55546VTR
EC-SIT-16	31	For fine tune USB3.0 quality: 1.Change U96 to PS8713BTQFN24GTR2-A3 2.DNS R4376/R4375/R4374/R4373/R4361/R4362 3..Staff R4367	1.Change U96 to PS8713BTQFN24GTR2-A3 2.DNS R4376/R4375/R4374/R4373/R4361/R4362 3..Staff R4367
EC-SIT-17	10	For fine tune X1/X2 Crystal accury 1.Change C1/C2/C3/C4 to 15pF	C1/C2/C3/C4

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